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MS-7B23

ATX:243.8mm*243.8mm

Ver: 1.0

Intel -CoffeeLake-S plamform

CPU:

LGA1151
CPU POWER PAK *4Phase
GT POWER PAK *2 Phase

System Chipset:

Cannon Lake B360

PWM:

VCORE - RT3606
DDR - RT8125E
DDR VPP25- MP2147
PCH(1.05V) - RT8125E
VCCSA - RT8125E
VCCIO - SY8288

Onboard Chip:

SIO: NCT5567D colay NCT5565D
HD Audio Codec: ALC887
LAN: RTL8111H
Flash ROM: SPI 64 MB
DP to VGA: RTD2167
CUT VBAT:SLG4B41231

Expansion Slots:

PCI Express (X16) Slot * 1
PCI Express (X1) Slot * 2
M.2 Slot * 2

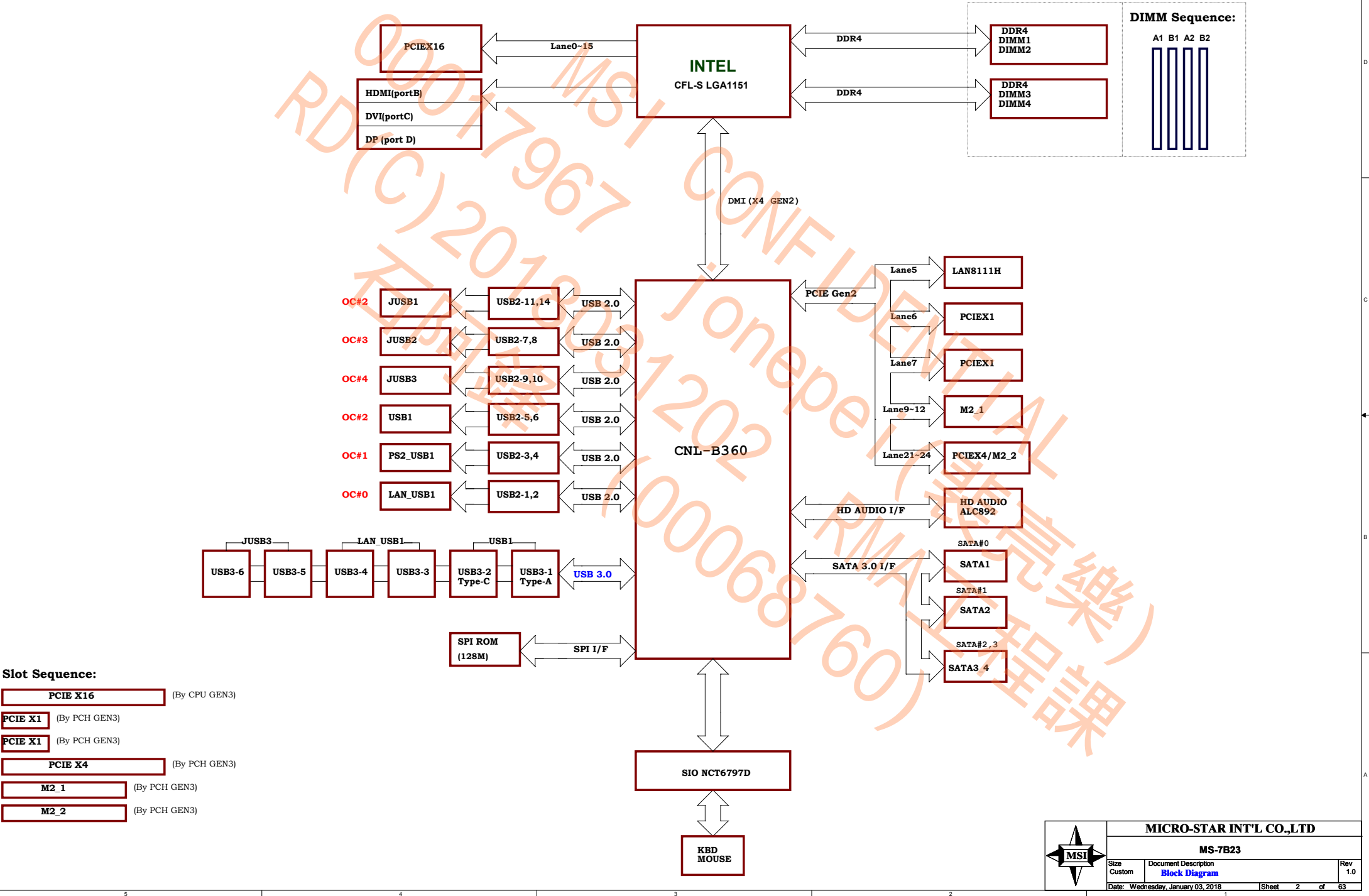
Main Memory:

DDR4 * 4 (Dual Channel)

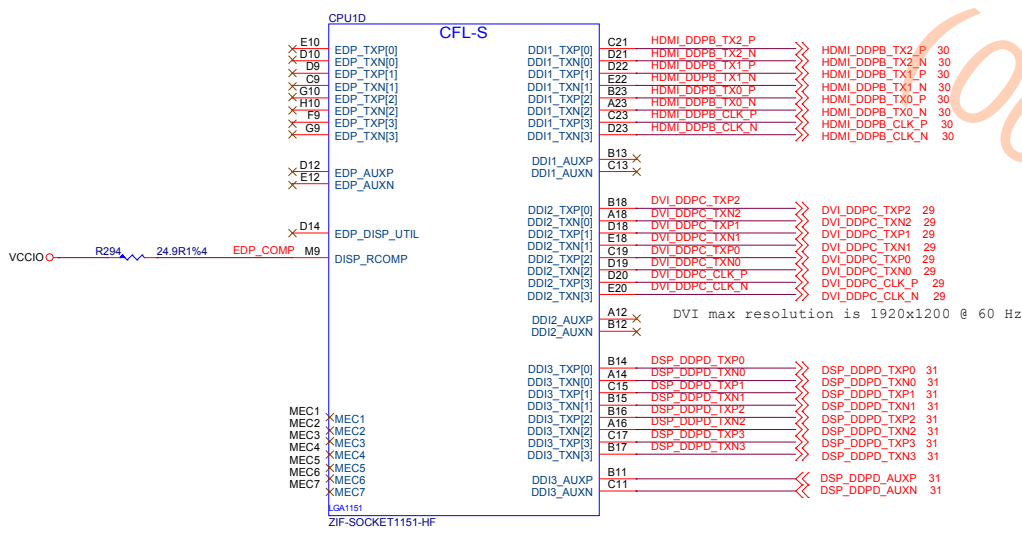
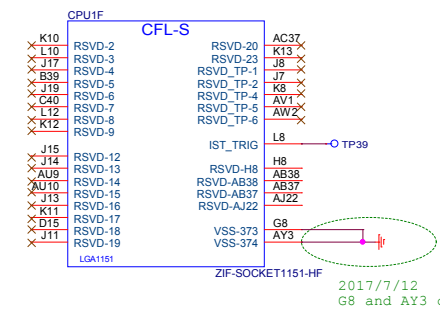
ACPI:

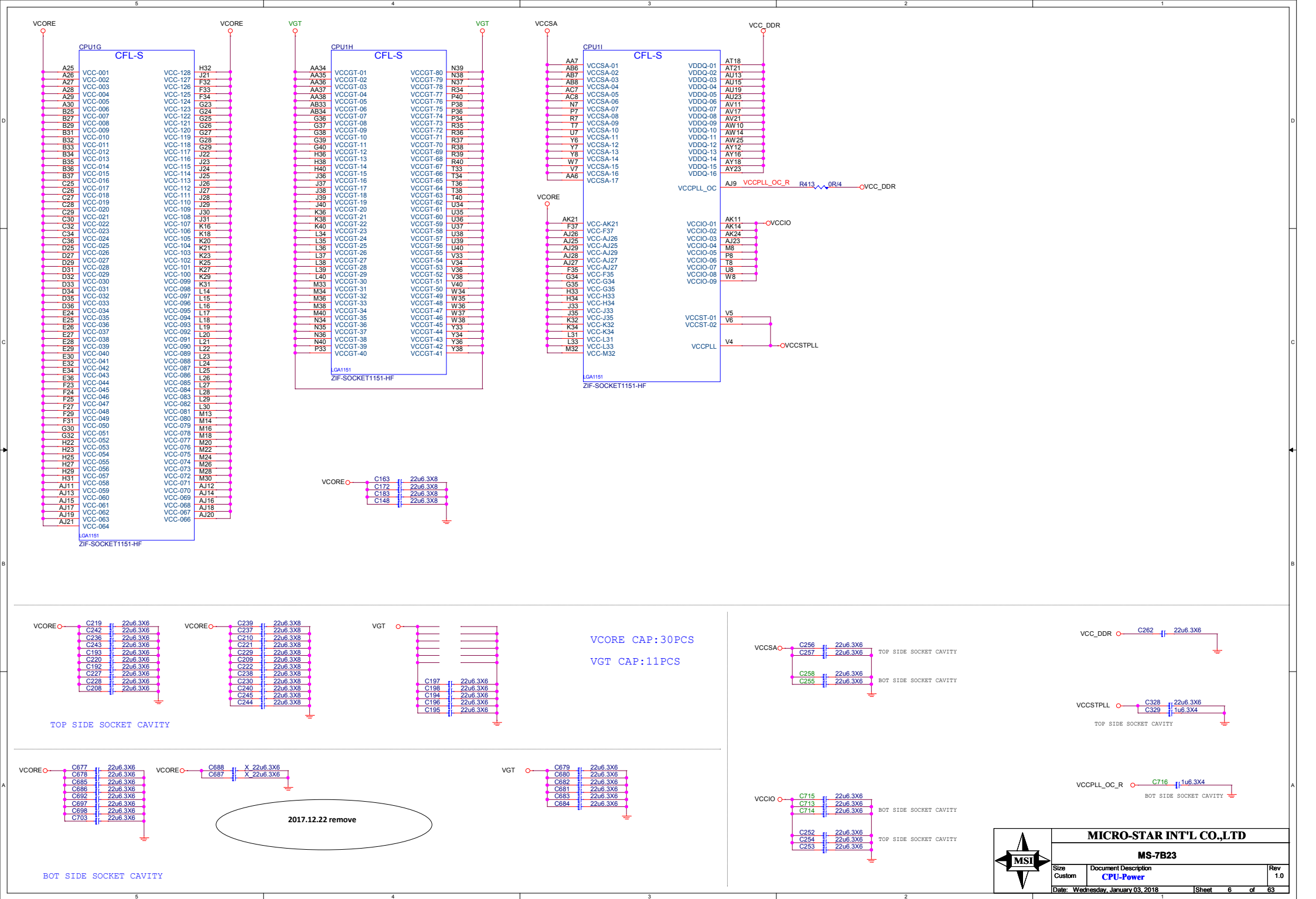
5VDAUL:uP7501
5VDIMM:uP7501
3VSB:GS7133+N MOS
1P8_VSB:GS7133
3VDSW:GS7116
VCCSTPLL:GS7133

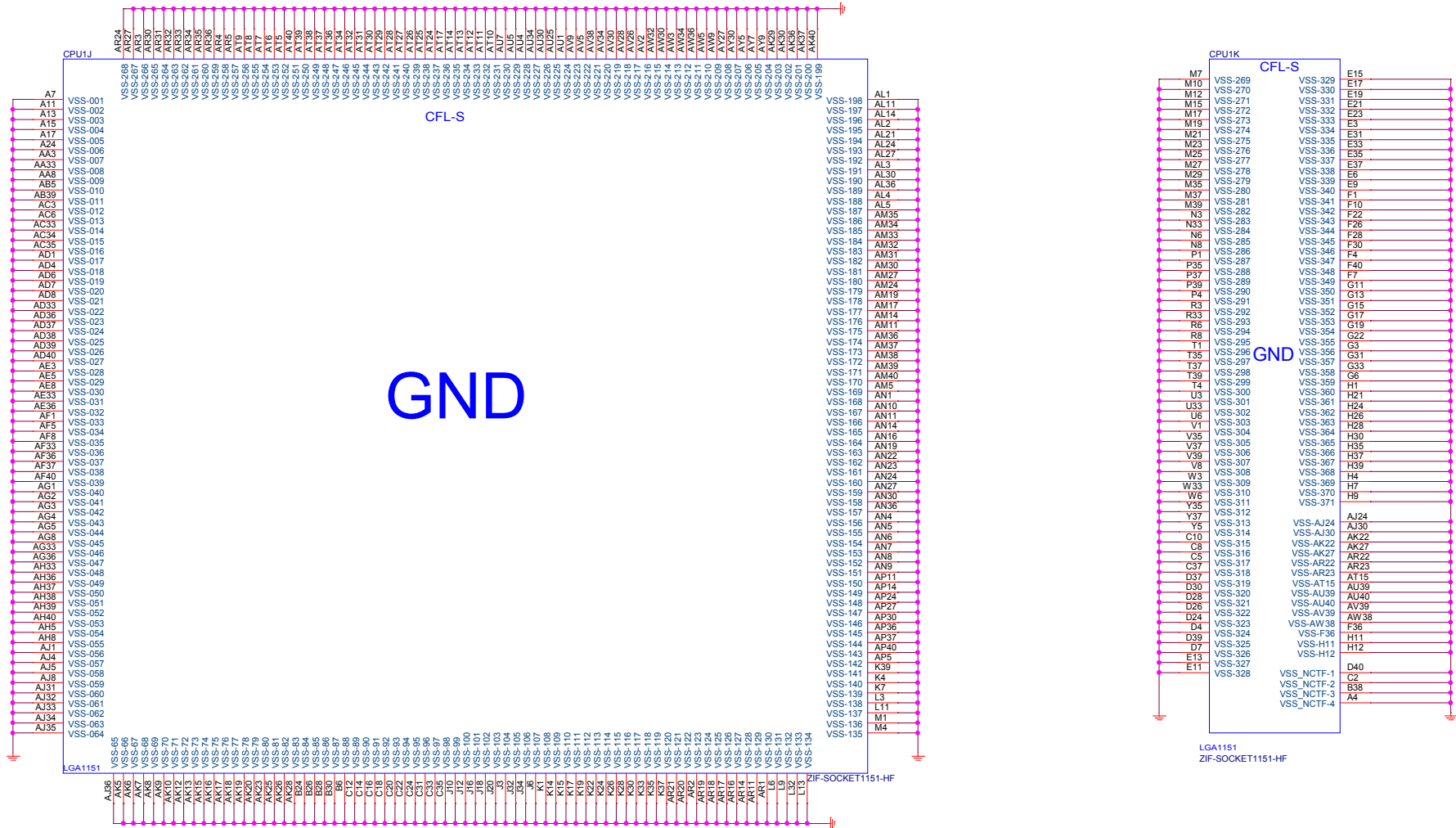
MS-7B23 Block Diagram

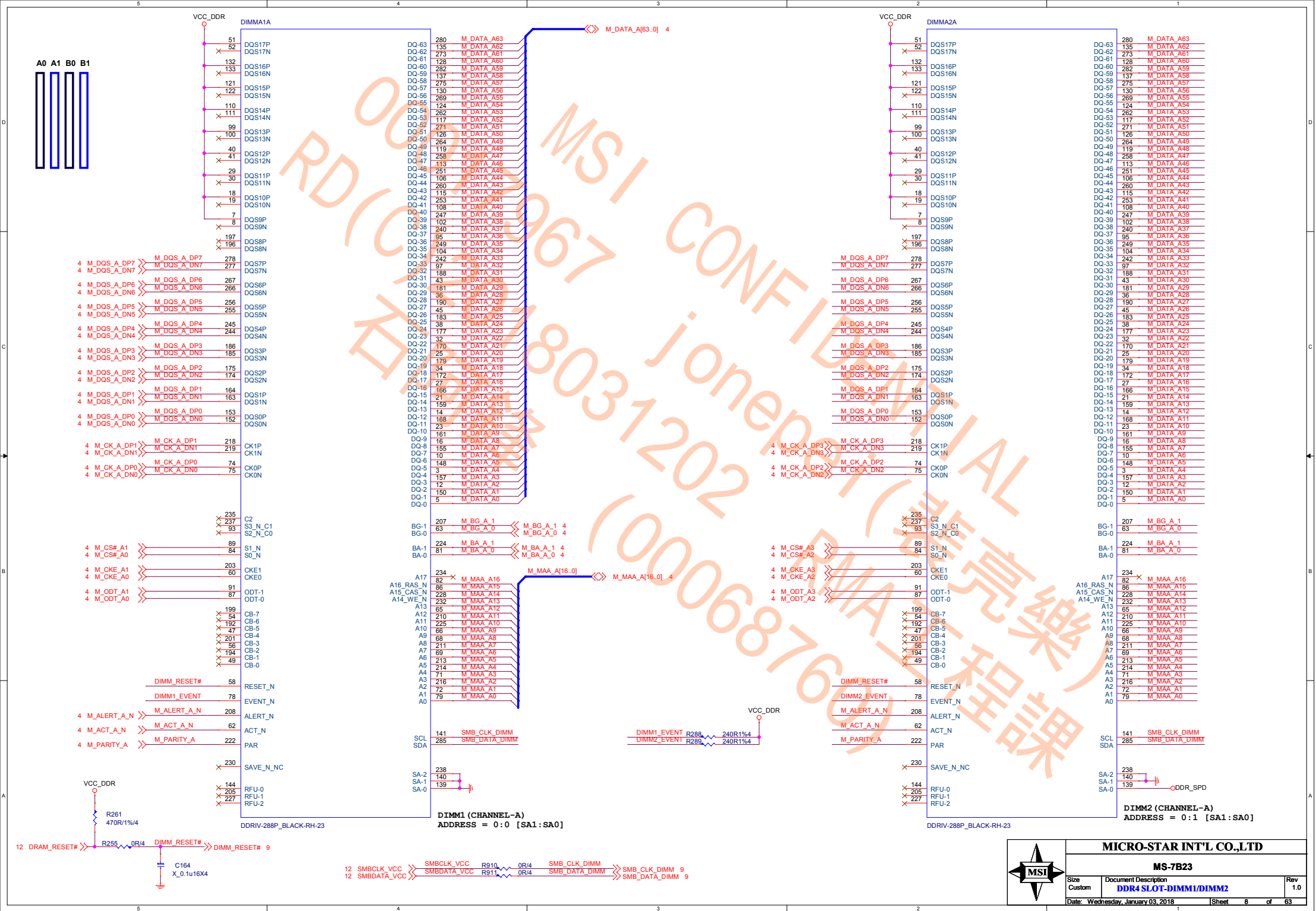


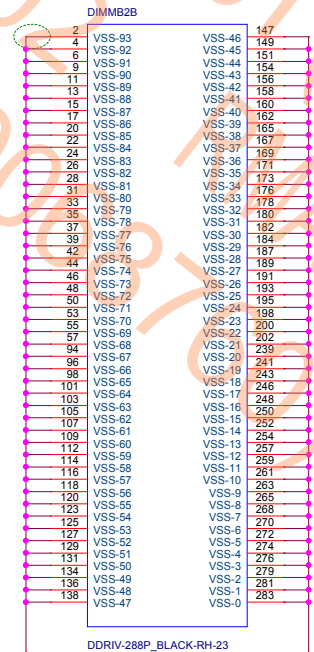
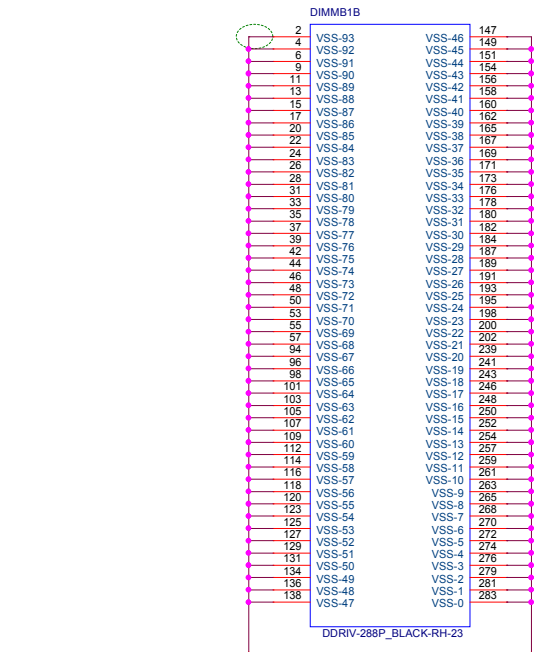
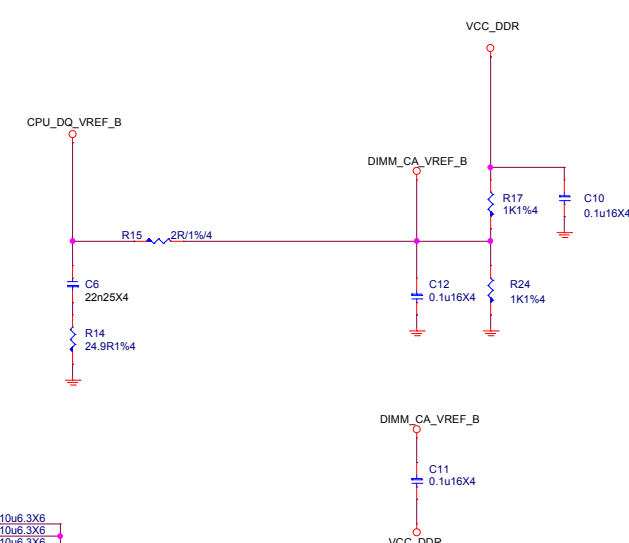
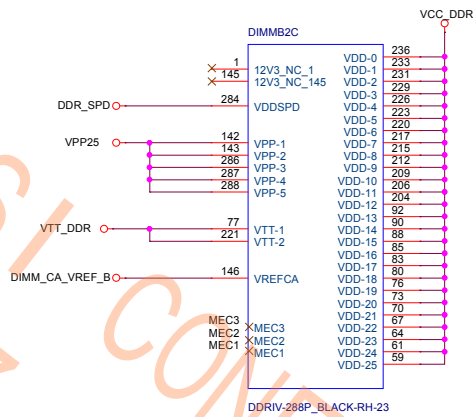
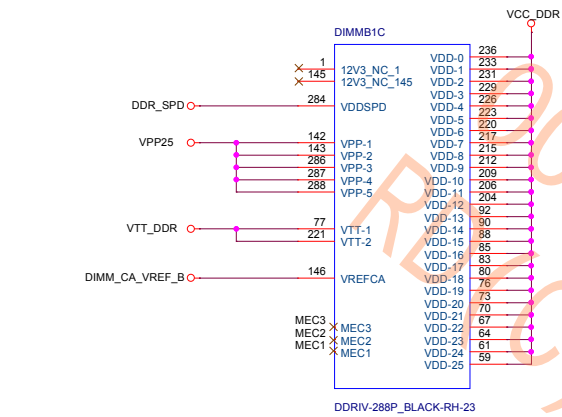




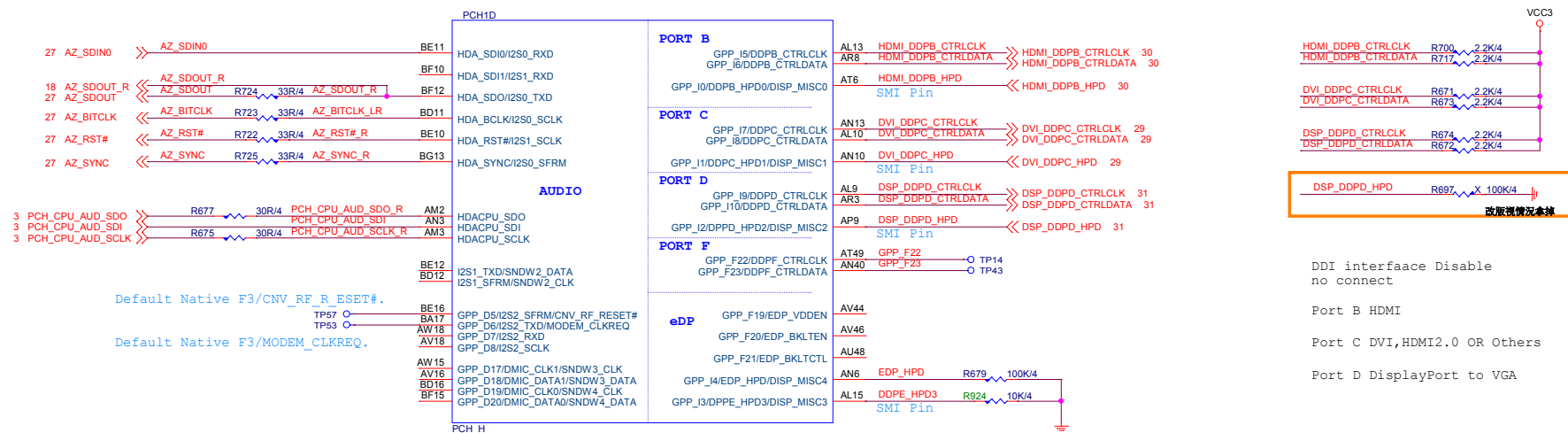
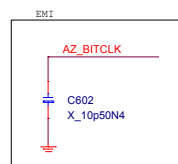
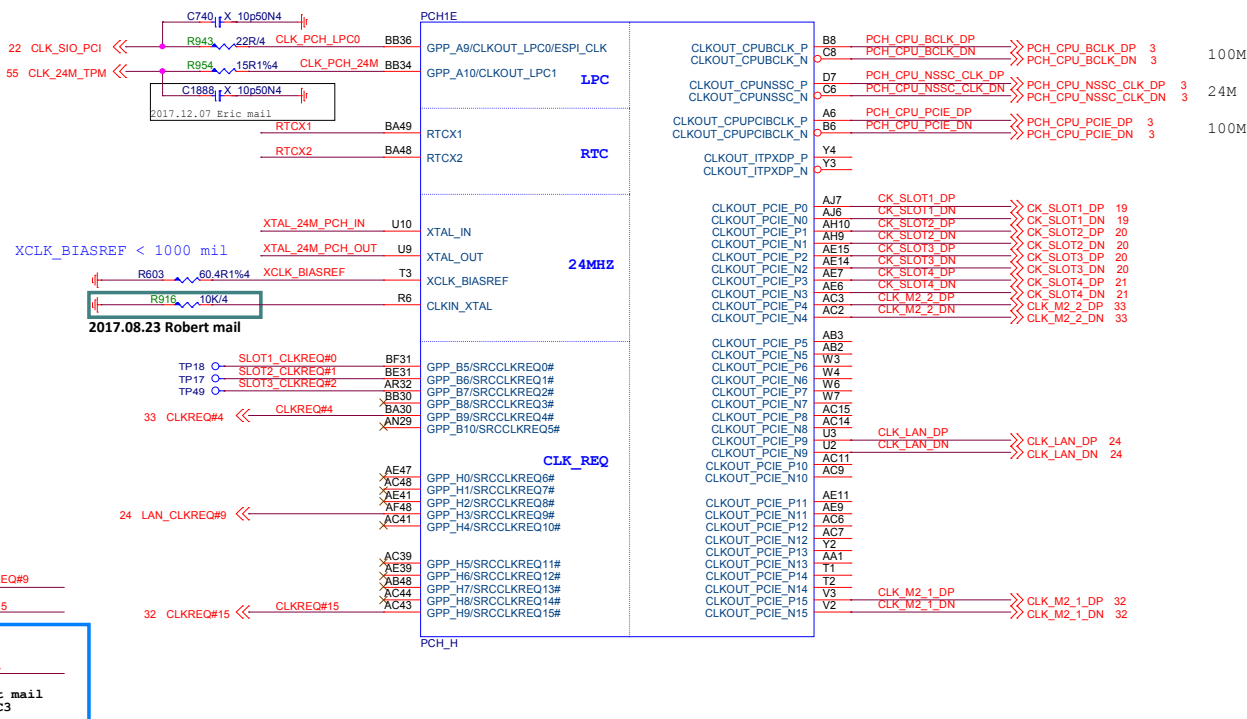
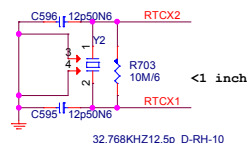








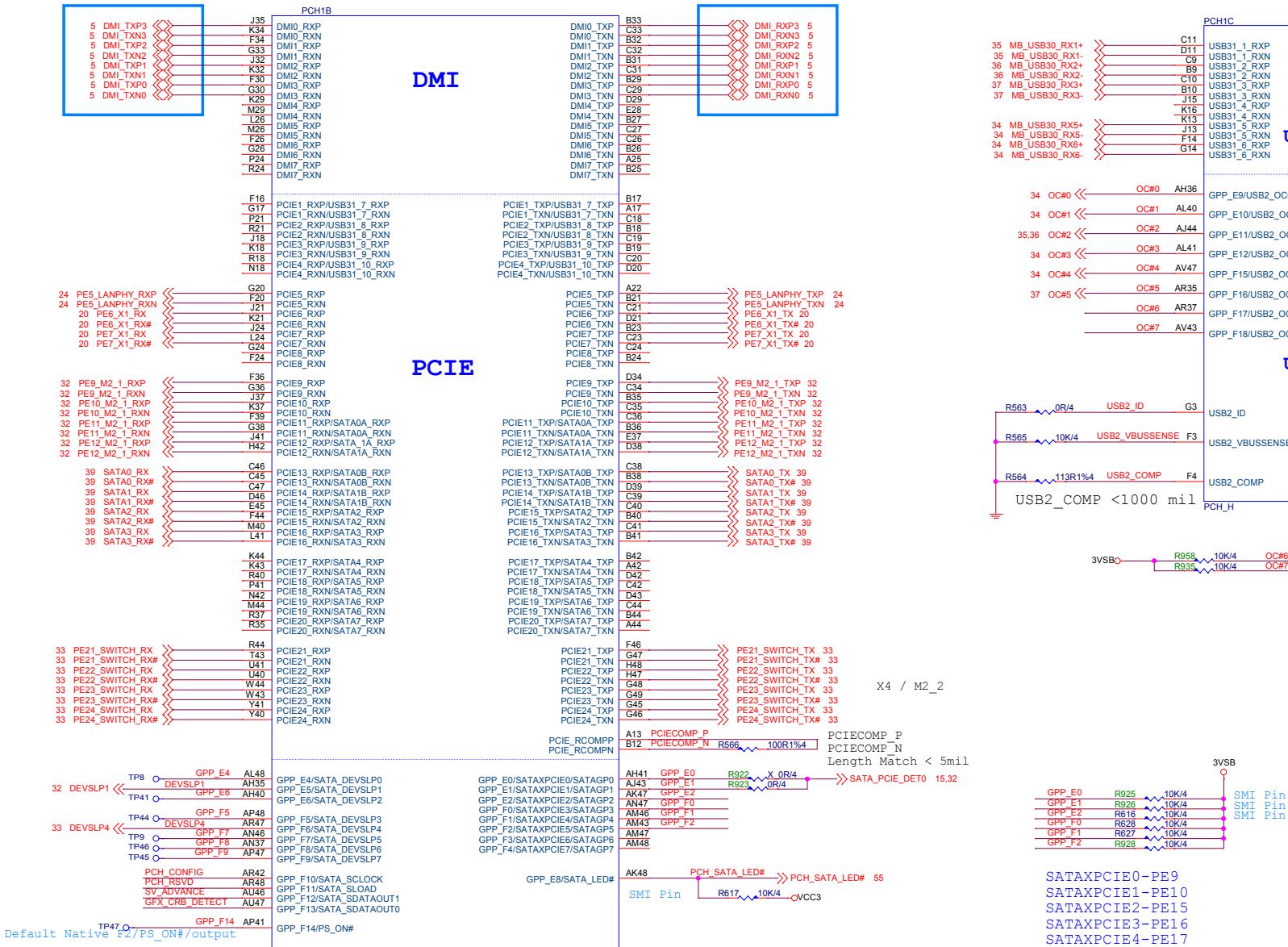
Close to PCH



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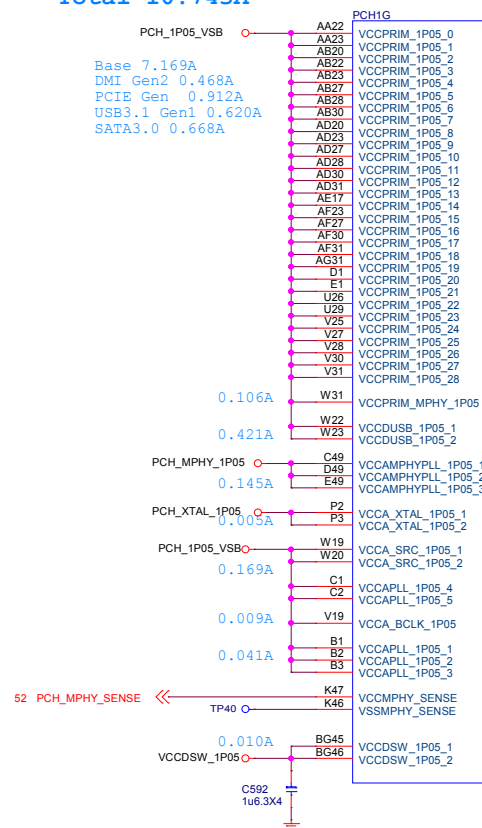
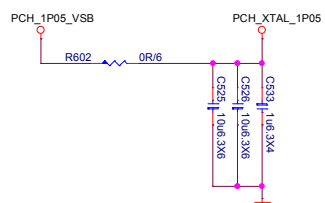
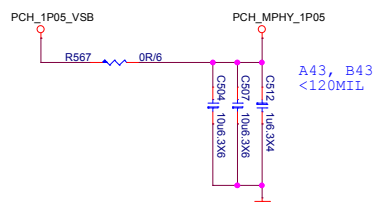
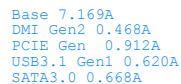
MS-7B23

Size	Document Description	Rev
Custom	PCB-USB/PCIE/DMI/SATA	1.0
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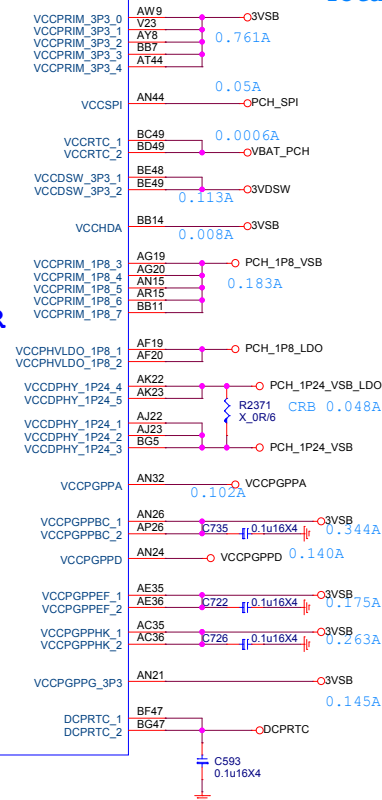
JTBT



MICRO-STAR INT'L CO.,LTD			
MS-7B23			
Size Custom	Document Description PCH-GPIO/USB0C/SATASTRAP		Rev 1.0
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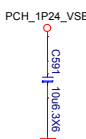
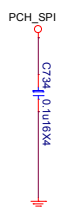
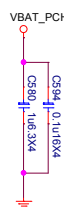
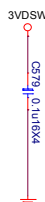
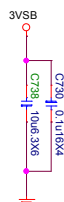
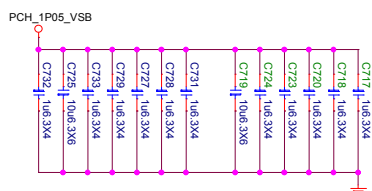
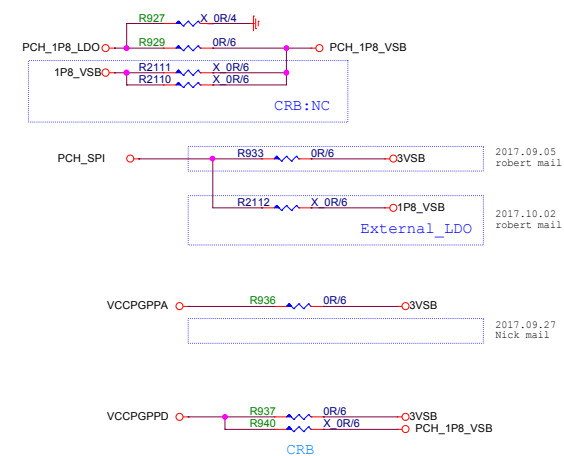


POWER



3VSB
Total 1.988A

PCH_1P8_VSB
Total 0.483A



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VSS

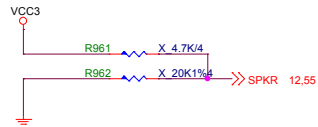


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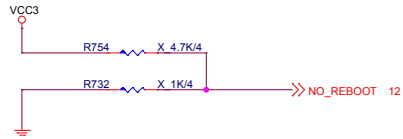
Size Custom	Document Description PCH-GND	Rev 1.0
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TOP Swap



Internal pull-down 20K is disabled after PLTRST#

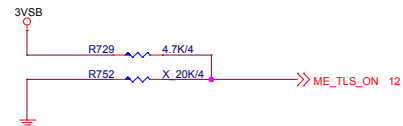
No Reboot



0 : DISABLE (Default)
1 : ENABLE

Internal pull-down 20K is disabled after PLTRST#

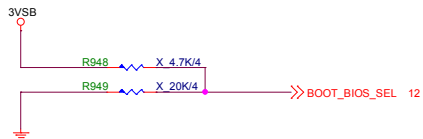
AMT and SBA with confidentiality



0 : DISABLE
1 : ENABLE (Default)

Internal pull-down 20K is disabled after RSMRST

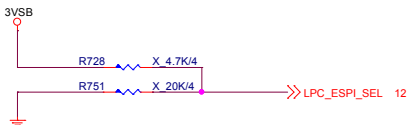
Boot BIOS



0 : SPI
1 : LPC

Internal pull-down 20K is disabled after PLTRST

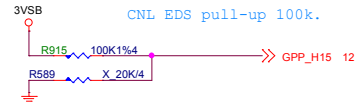
LPC eSPI Mode



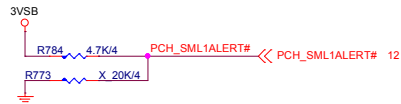
0 : LPC
1 : eSPI

Internal pull-down 20K is disabled after RSMRST

Reserved



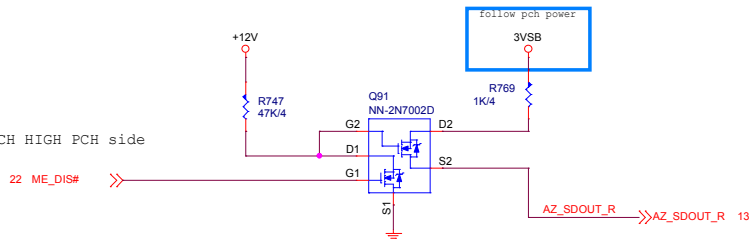
Reserved



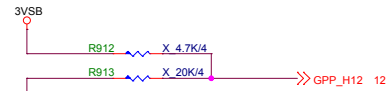
HDA_SDO

ME flash by GPIO

PCH HIGH PCH side



ESPI FLASH SHARING MODE

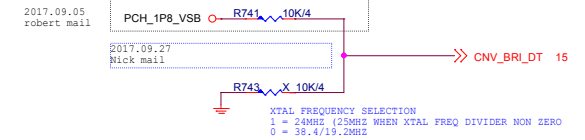
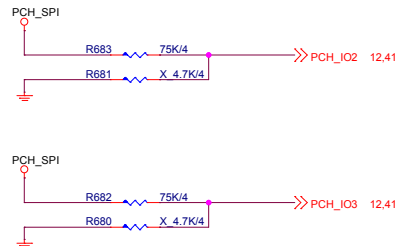


0 : MASTER ATTACHED FLASH SHARING
1 : SLAVE ATTACHED FLASH SHARING

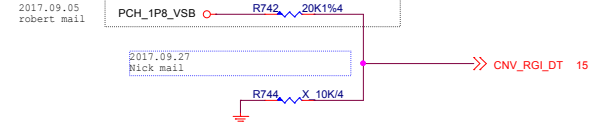
Internal pull-down 20K is disabled after RSMRST

Reserved

CRB 571506 Page.99

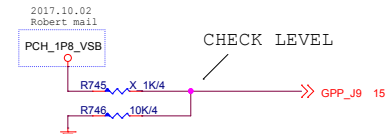


XTAL FREQUENCY SELECTION
1 = 24MHz (25MHz WHEN XTAL FREQ DIVIDER NON ZERO)
0 = 38.4/19.2MHz



CNL EDS
0 = Integrated CNVi enable
1 = Integrated CNVi disable

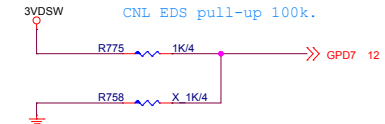
1.8V VCCPSPI



VCCPSPI 3.3V, Internal pull-down.

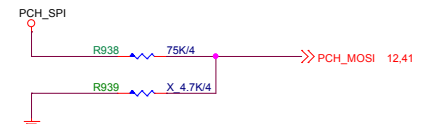
SELECT THE SPI BIOS FLASH INTERFACE OPERATING VOLTAGE
0 = VCCPSPI IS CONNECTED TO 3.3V RAIL - DEFAULT
1 = VCCPSPI IS CONNECTED TO 1.8V RAIL
PCH HAS INTERNAL 20K PD

Reserved

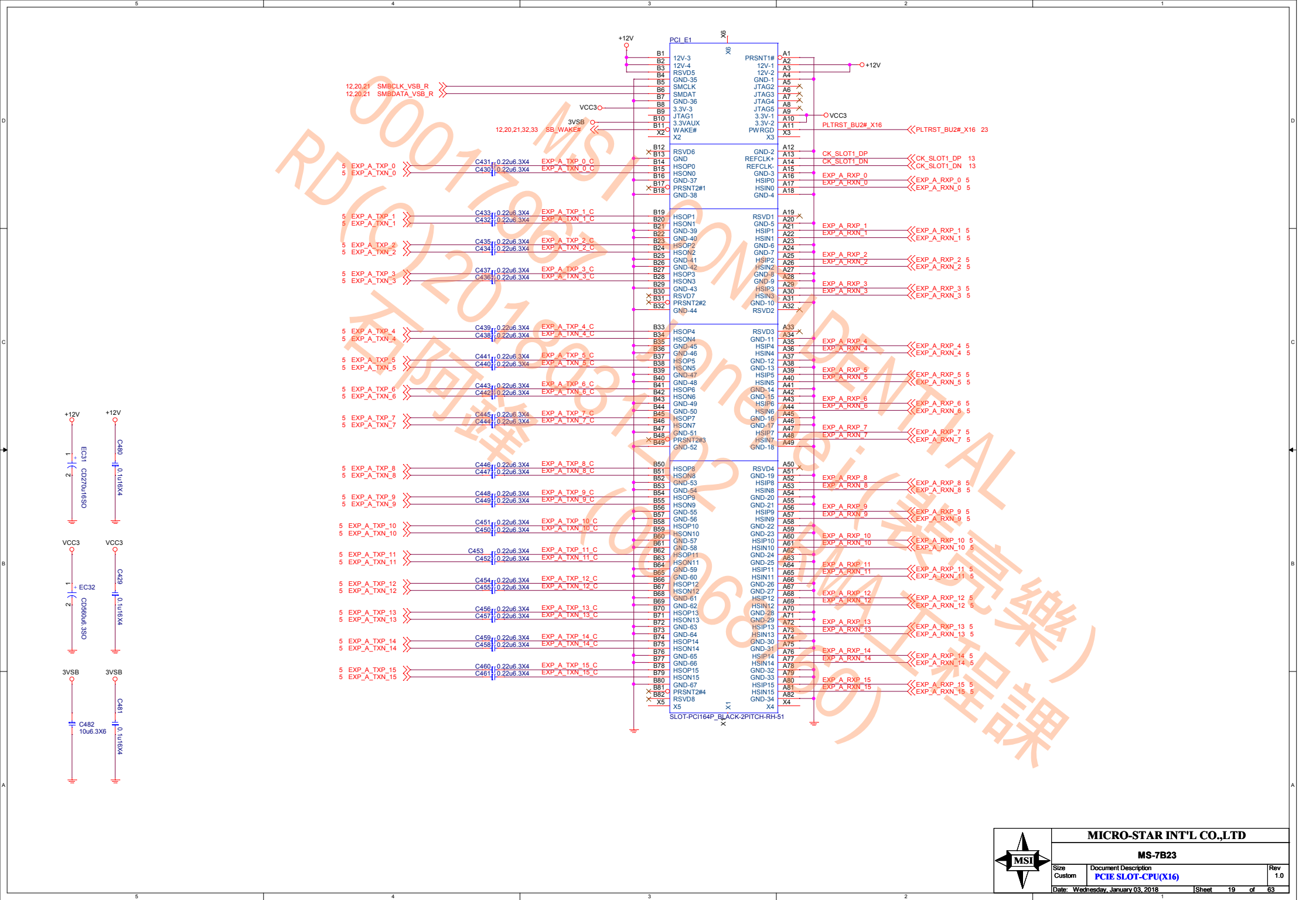


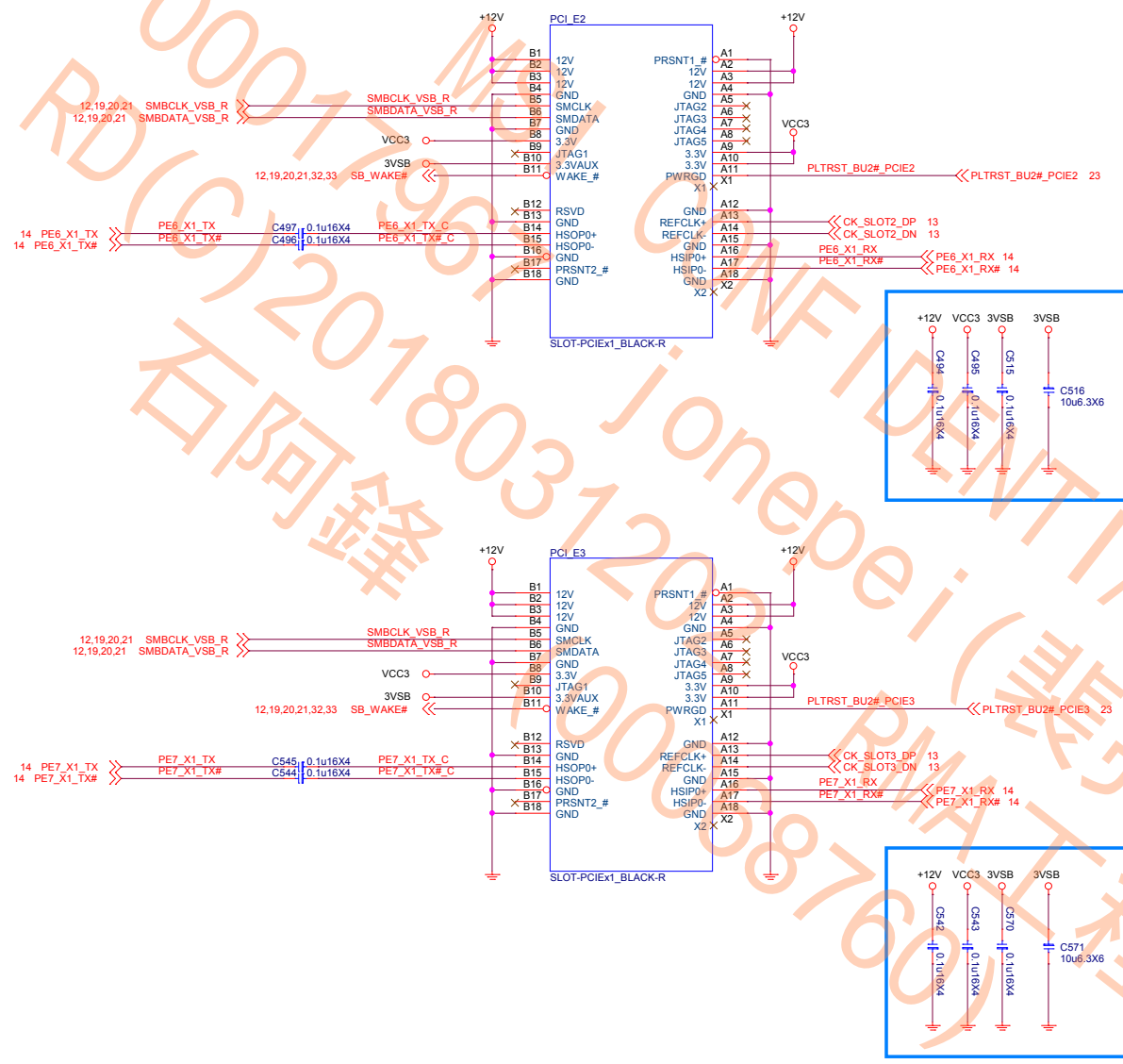
XTAL INPUT MODE
0 = XTAL INPUT IS SINGLE-ENDED
1 = XTAL INPUT IS DIFFERENTIAL
PCH HAS INTERNAL 20K PD

Reserved



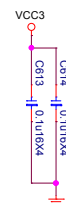
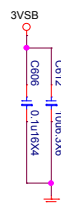
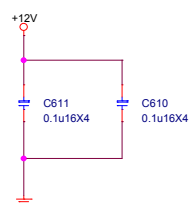
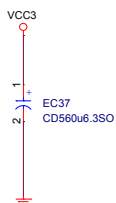
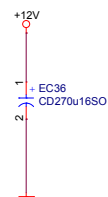
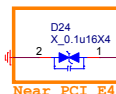
MICRO-STAR INT'L CO.,LTD			
MS-7B23			
Size	Document Description	Rev	
Custom	PCH-Strap	1.0	
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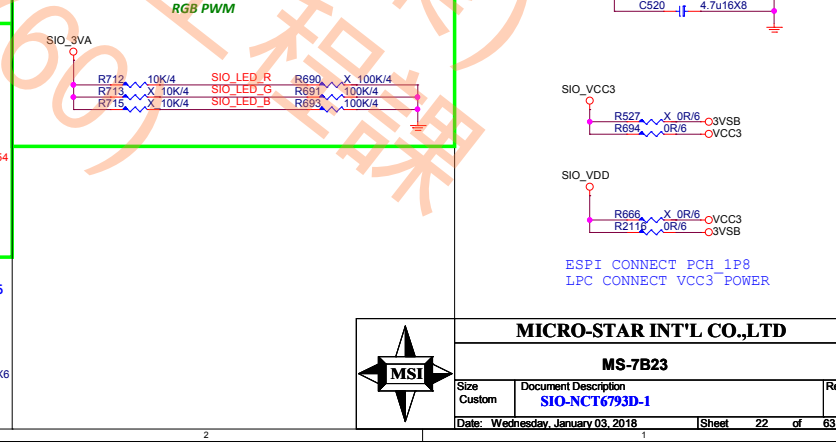
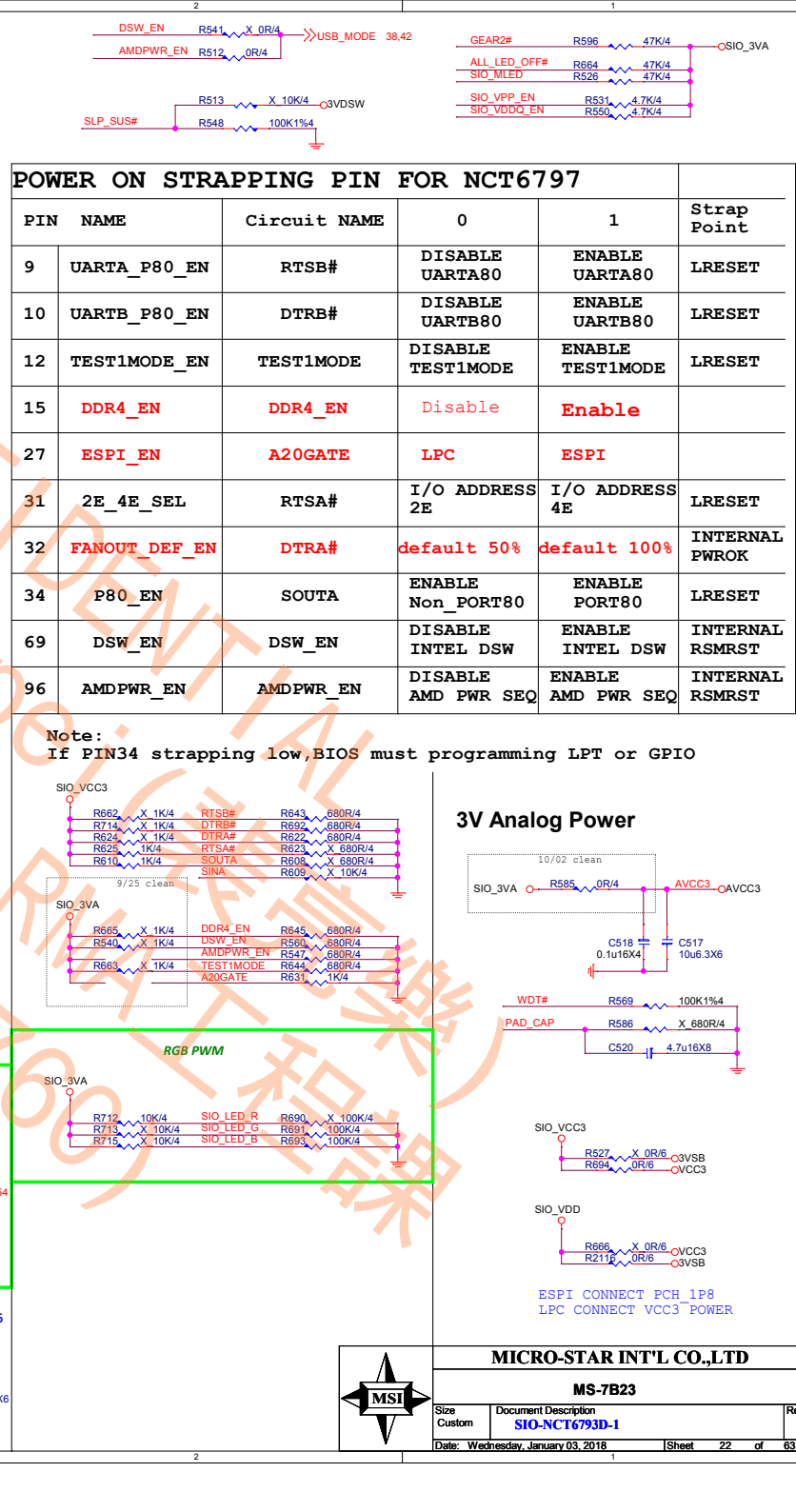
MICRO-STAR INT'L CO.,LTD		
MS-7B23		
Size	Document Description	Rev
Custom	PCI SLOT-PCH(XI)	1.0
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Near PCI E4

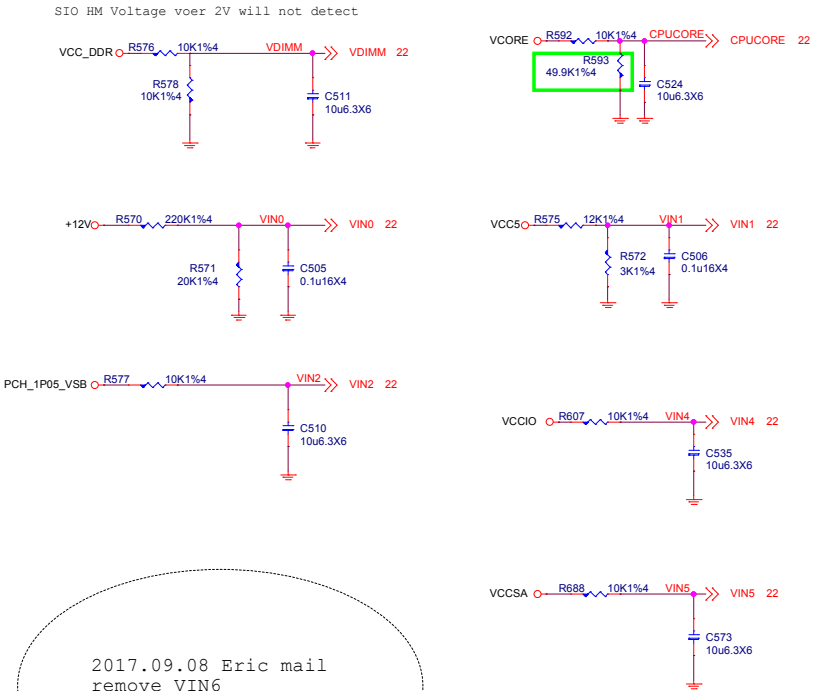


MS-7B23

Size Custom	Document Description PCIE SLOT-PCH(X4)	Rev 1.0
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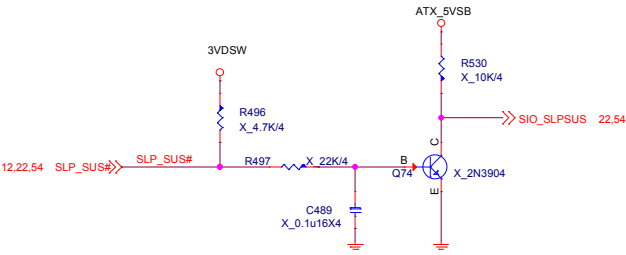


HW Monitor - Voltage



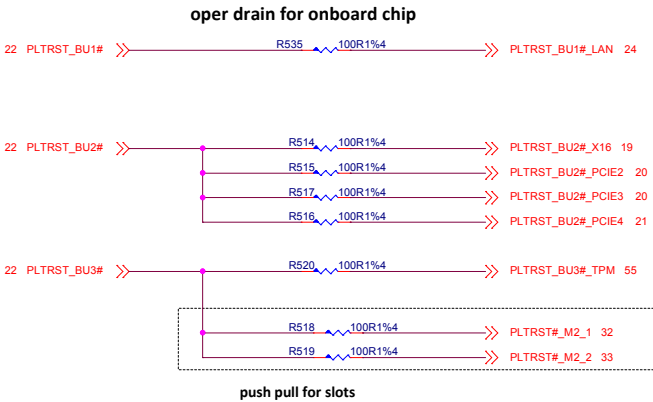
2017.09.08 Eric mail
remove VIN6
change to AUXTIN2

SLP_SUS Co-lay circuit



2017.09.25
remove for space

PLTRST#

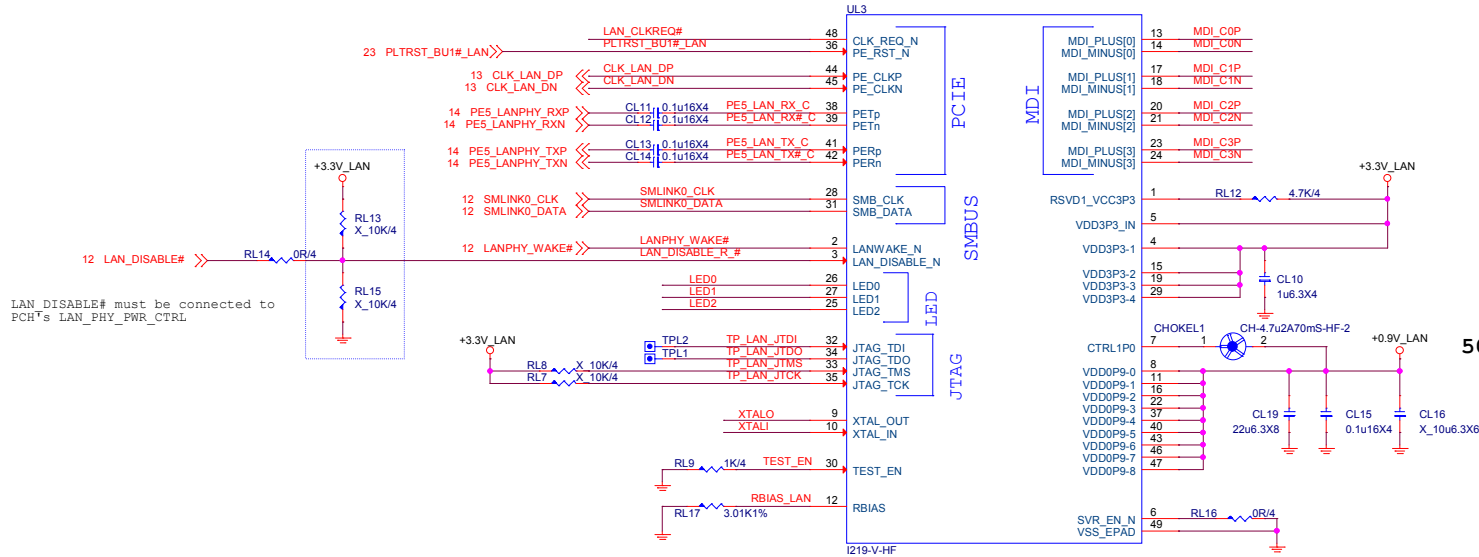


SERIAL PORT 1

2017.09.25
remove JCOM1

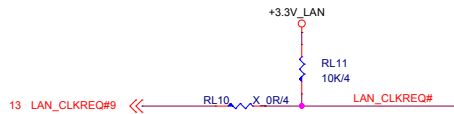
Intel Lan- i219

8111H:B06-08111CC-R09
8111G:B06-081116C-R09

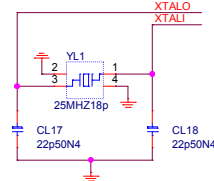


LAN_DISABLE# must be connected to PCH's LAN_PHY_FWR_CTRL

PCH's PCIECLKRQ<n> port must be mapped to PCH's PET/R<n+1>port. If CLK_REQ_N is not used, pin48 is pulled up 10K to 3.3V_LAN

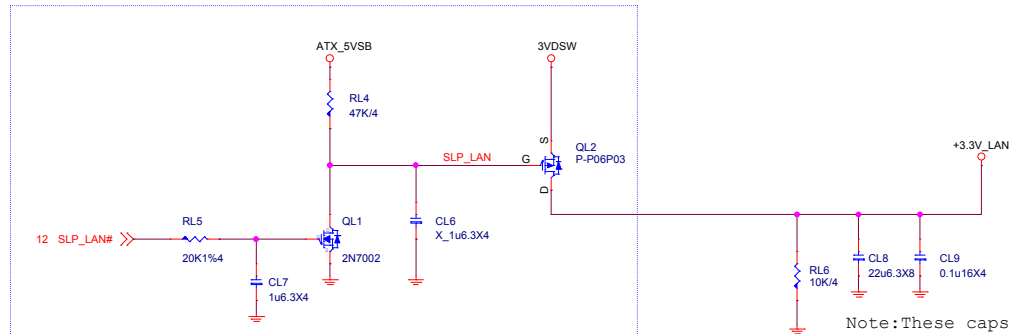


AVL:D04-1005700-SC6



The 10Kohm pull-up resistor (RL18) of CLK_REQ_N is connected to 3.3V Suspend/Core/etc. power well, depending on the power well of PCH's input PCIECLKRQ<n> buffer.

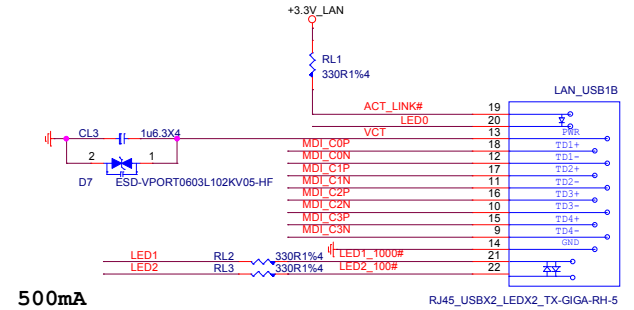
support WOL from Deep Sx:
Power source from 3VA (DSW power) & make sure MAX current is enough to support i218/i219.



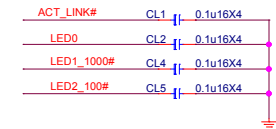
Note: These caps closed to PHY

+3.3V LAN
I218: 132mA
I219: 542mA

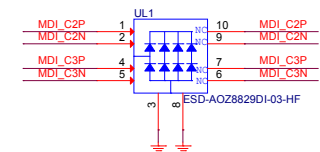
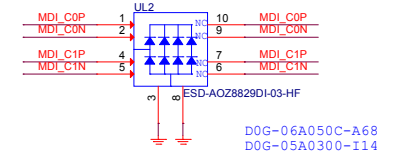
LAN Connector



For EMI



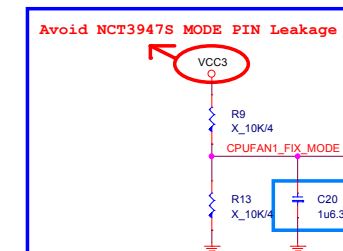
UL2&UL3 close to connector



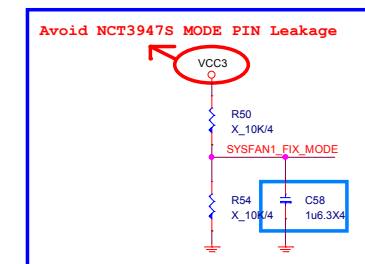
Do not pair MDI0 and MDI1 on the same TVS device (avoid LAN POE connecting issue). Other pairing combination is ok.

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Custom	LAN - Intel I219	1.0	
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2.GPIO可以由BIOS切换 PWM/DC MODE



2.GPIO可以由BIOS切換 PWM/DC MODE

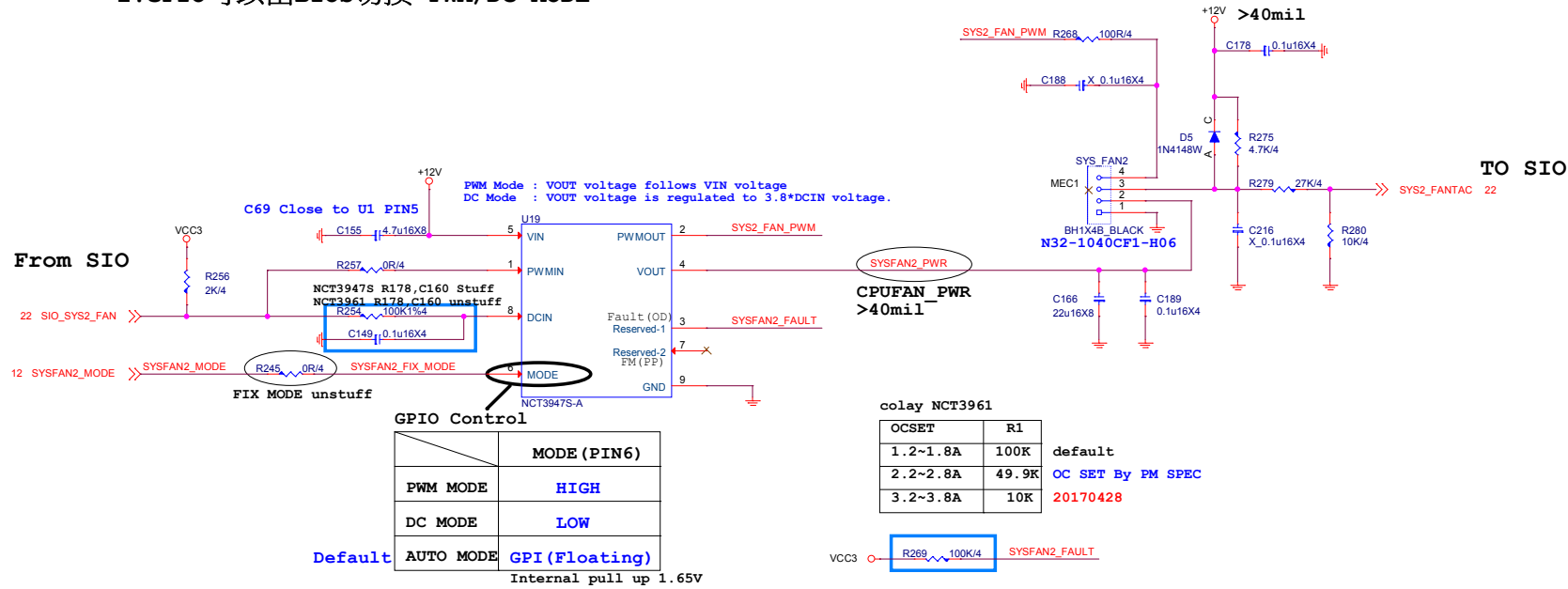


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Size Custom	Document Description FAN CONTROLLOR	Rev 1.0
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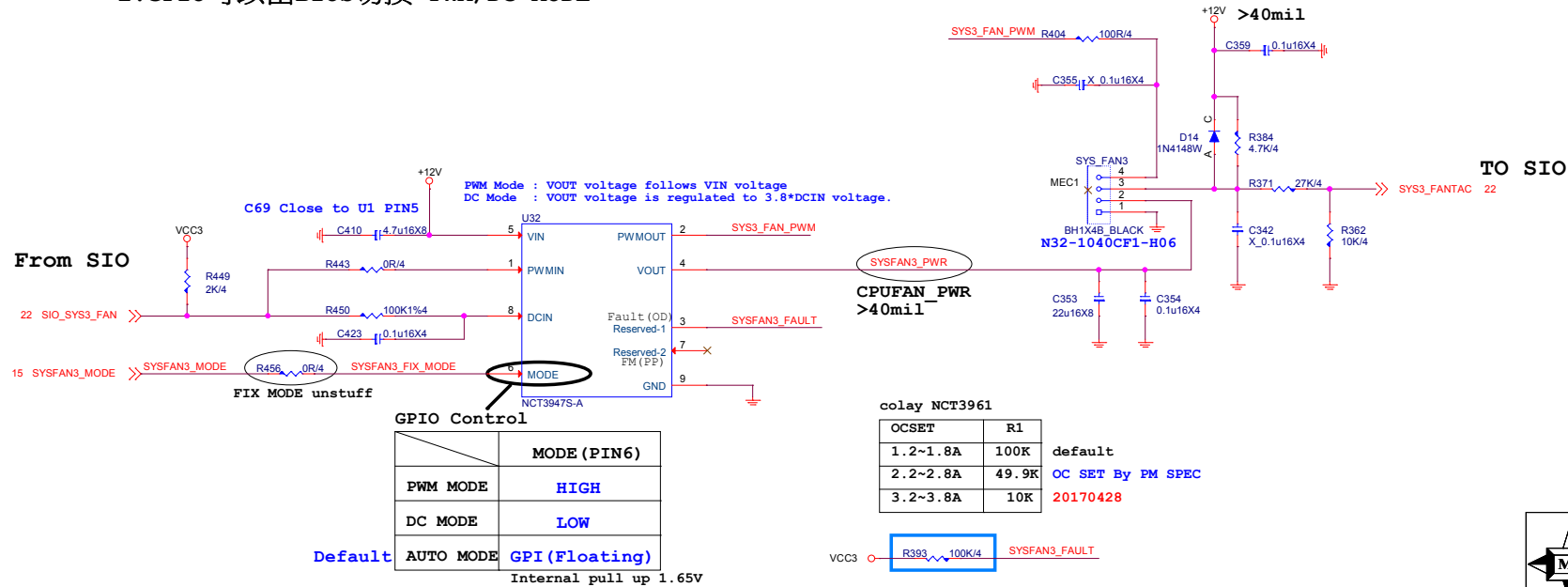
TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

2.GPIO可以由BIOS切换 PWM/DC MODE



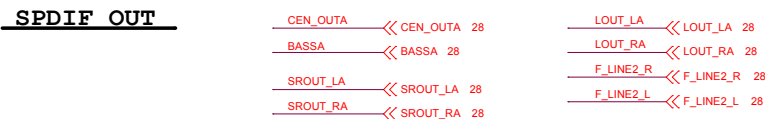
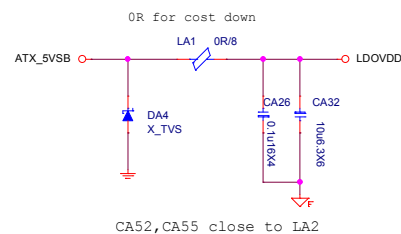
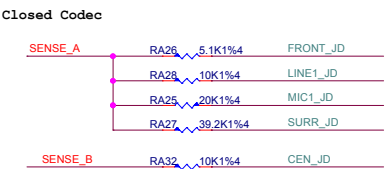
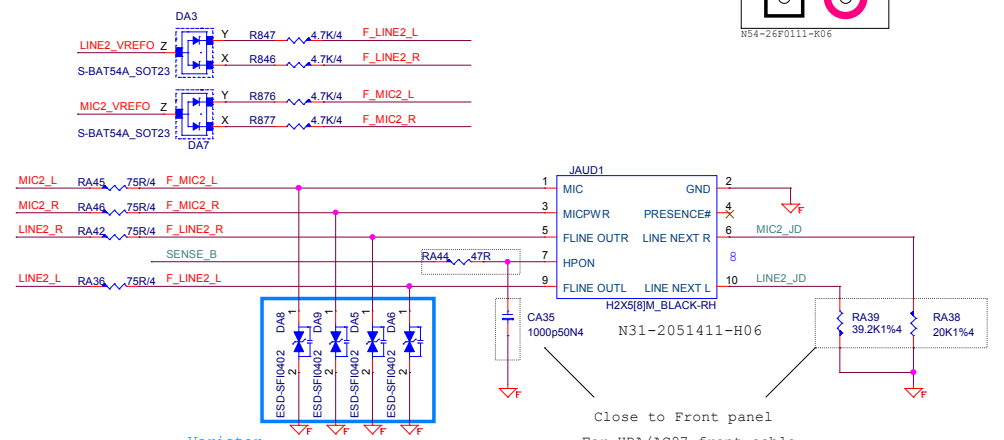
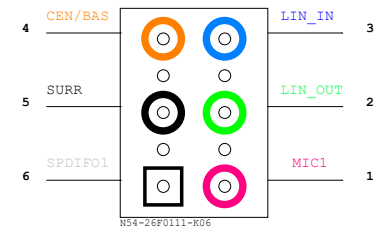
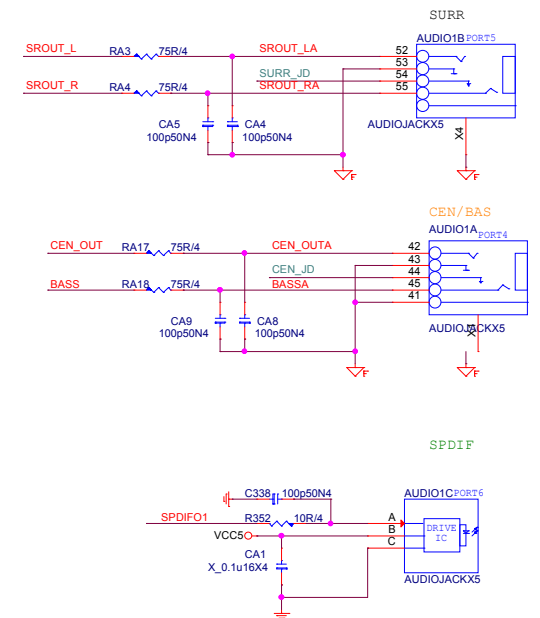
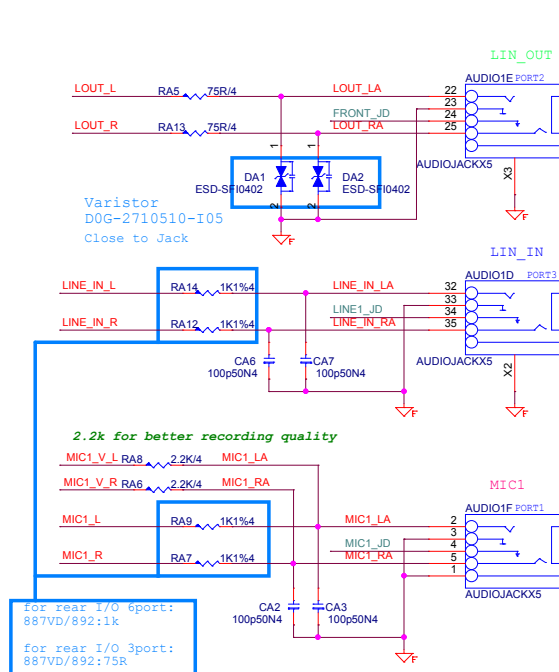
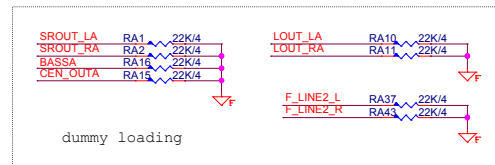
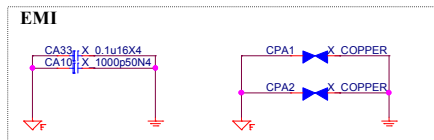
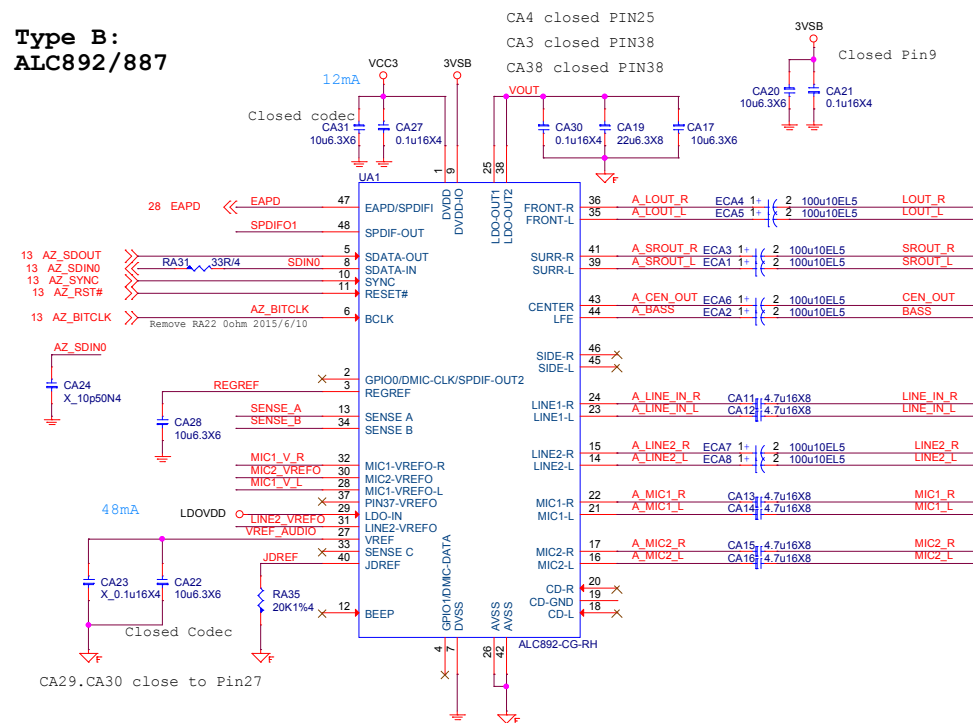
TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

2.GPIO可以由BIOS切换 PWM/DC MODE



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Type B:
ALC892/887



MICRO-STAR INT'L CO.,LTD

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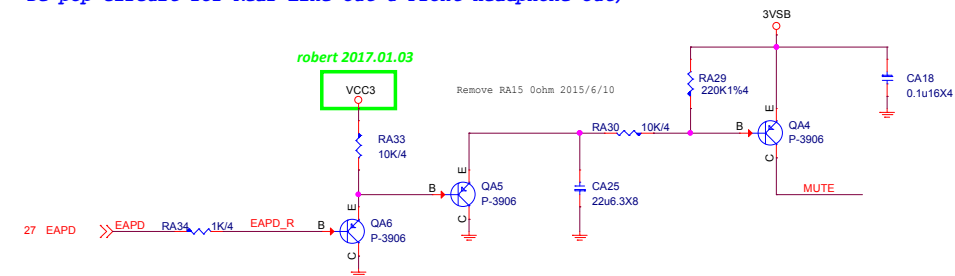
Date: Wednesday, January 03, 2018		Sheet 27 of 63	
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Rear Line OUT De-POP circuit

De-pop circuit for Rear Line out & Front Headphone out)

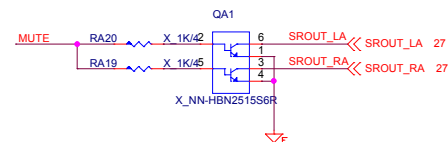
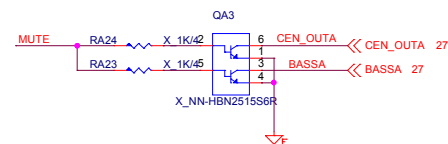
(add de-pop circuit by PM spec or customer request,
NOTE: add de-pop circuit need to change CA21,CA37, CA38, CA39, CA40, CA41 to TVS)

robert 2017.01.03

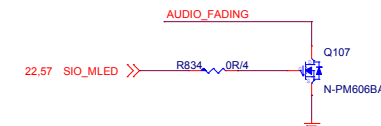
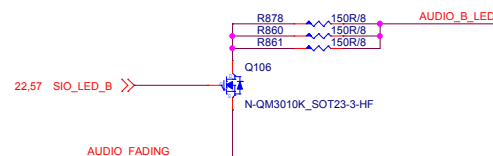
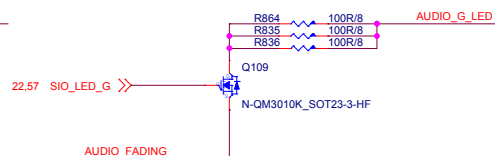
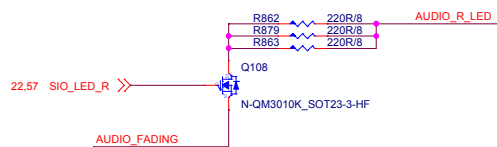
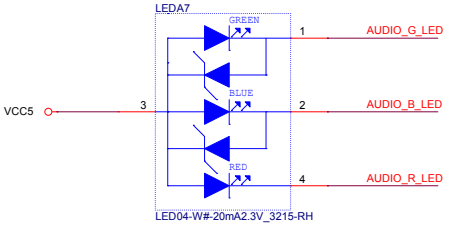
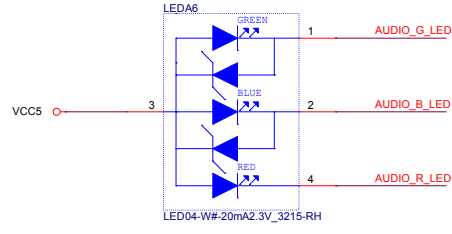
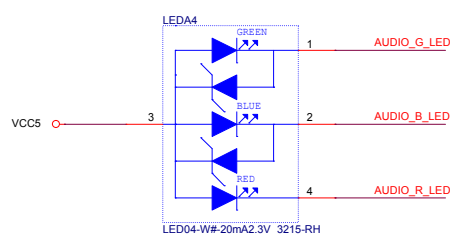
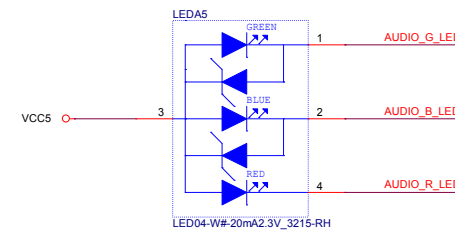
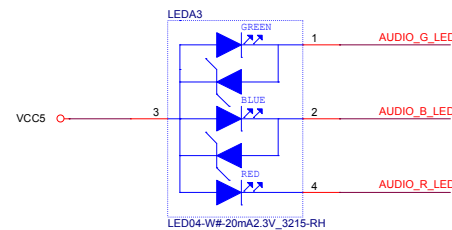
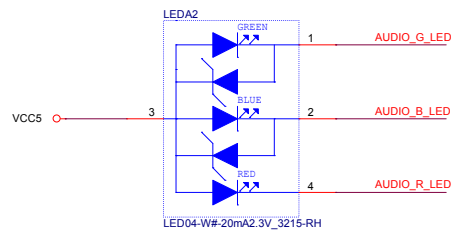
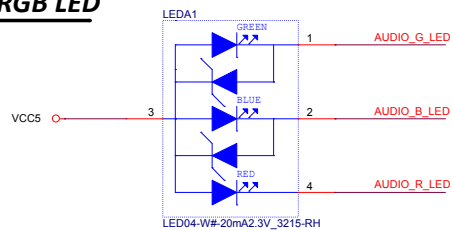


Digital

Analog



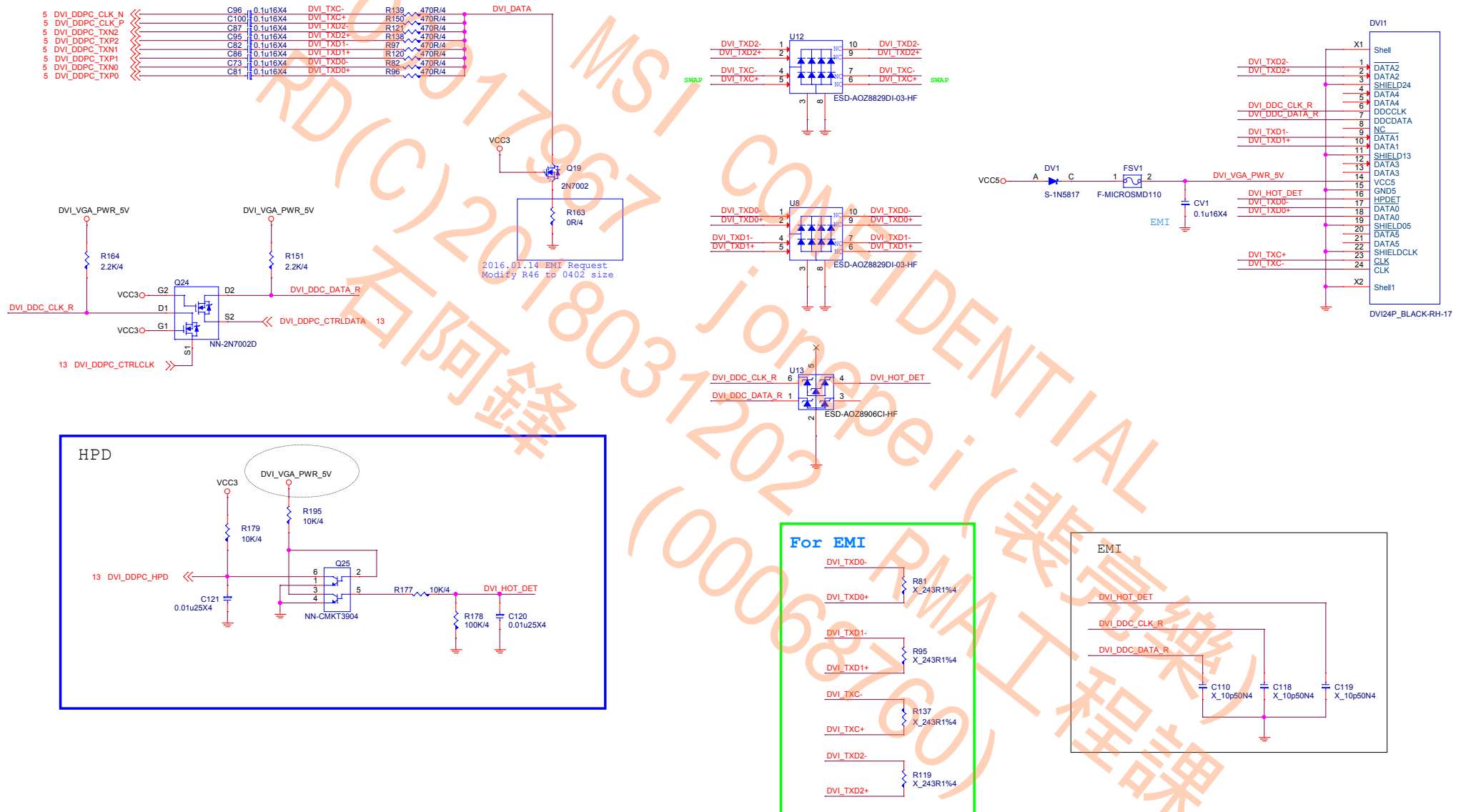
Audio RGB LED



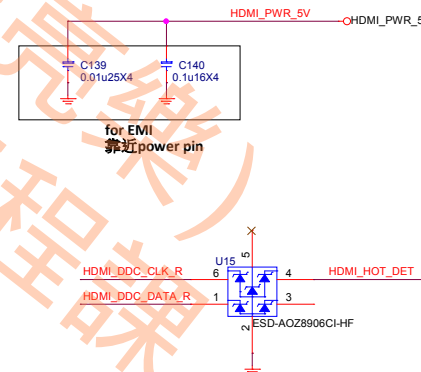
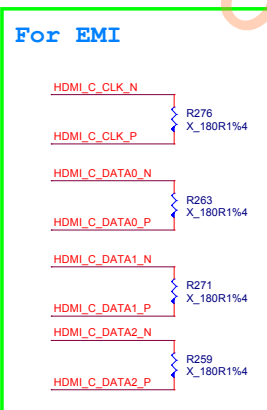
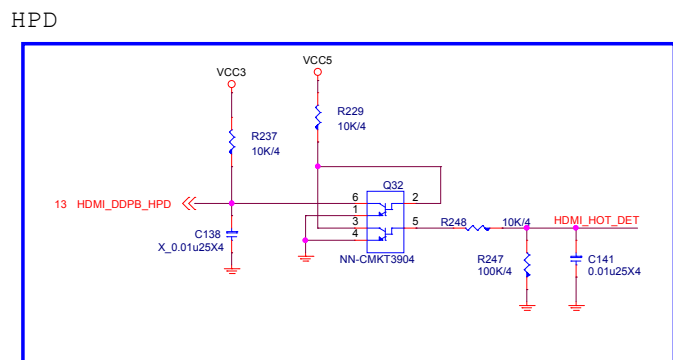
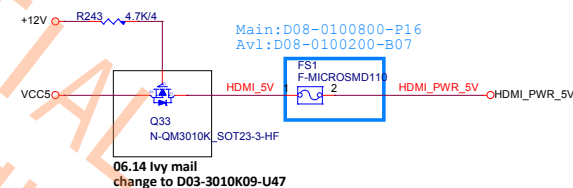
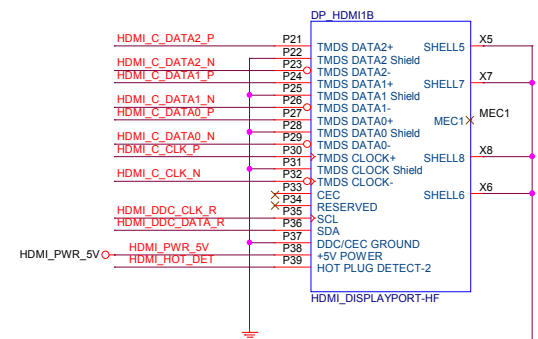
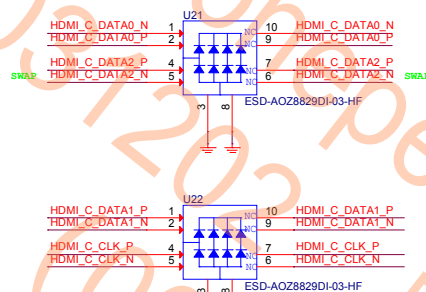
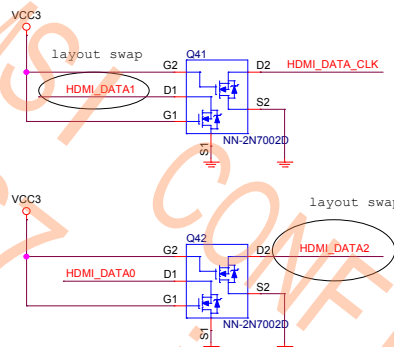
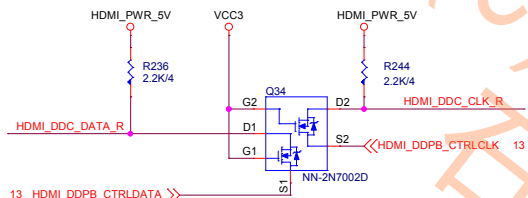
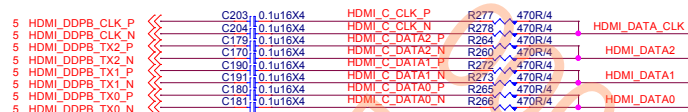
MICRO-STAR INT'L CO.,LTD			
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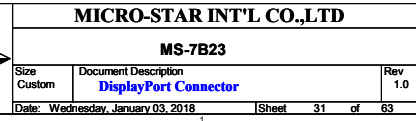
DVI level shifter

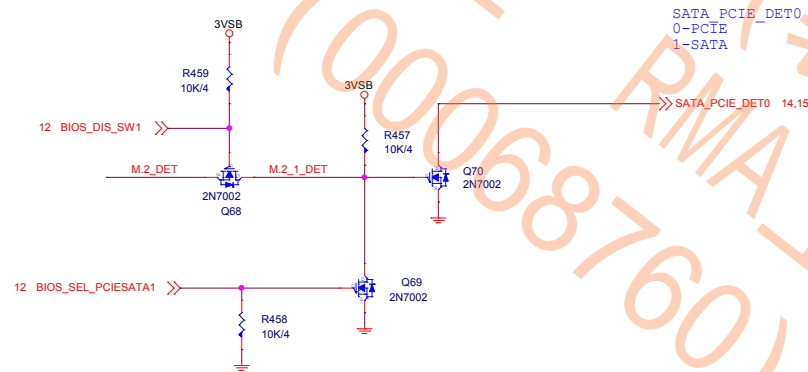
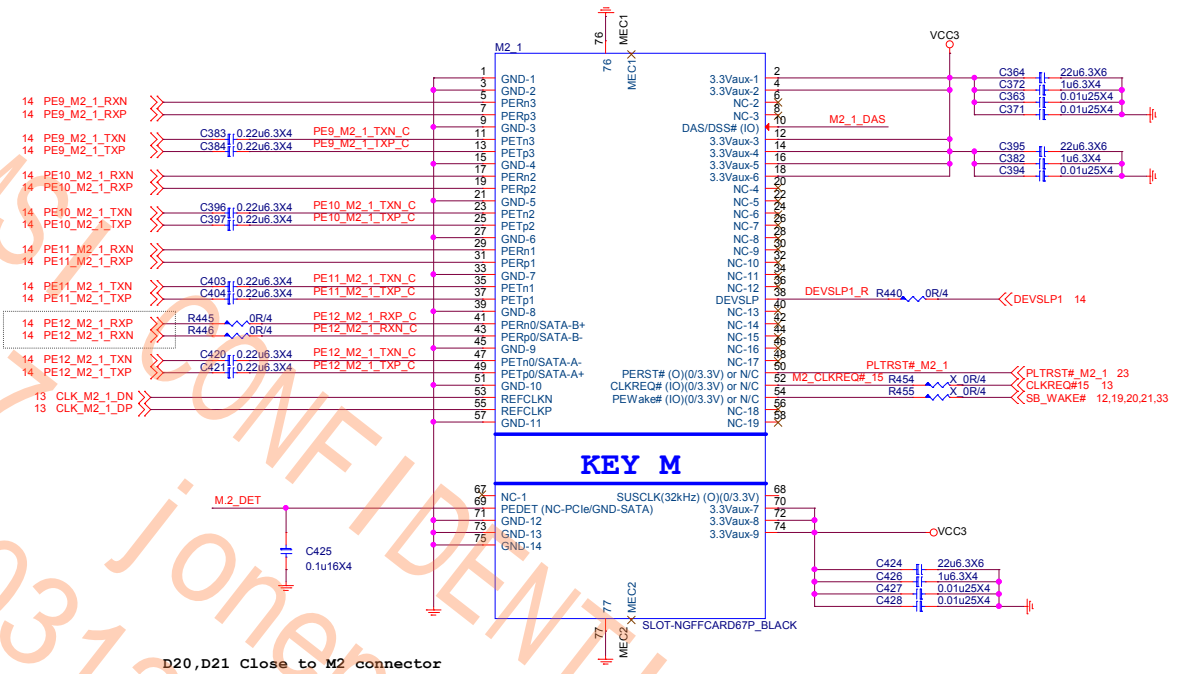
VGA: resolution of 2048x1536 pixels with 32-bit color at 75 Hz (4:3 QXGA)



HDMI, DVI : 1920x1200 at 60 Hz (16:10 WUXGA)

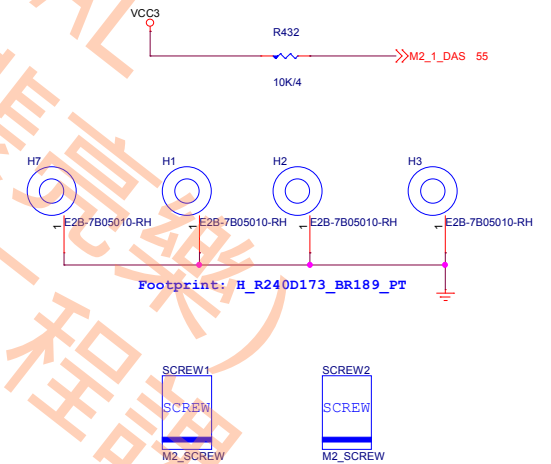






BIOS_MODE

DIS_SW	M1_SEL_PCIESATA	Mode
0	1	M2-SATA
0	0	M2-PCIE
GPI	GPI	AUTO

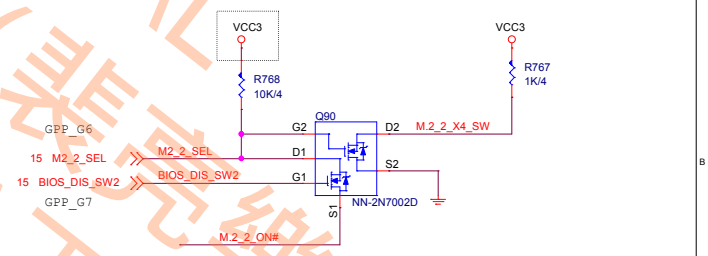
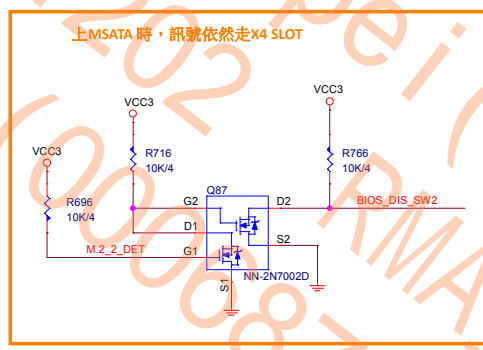
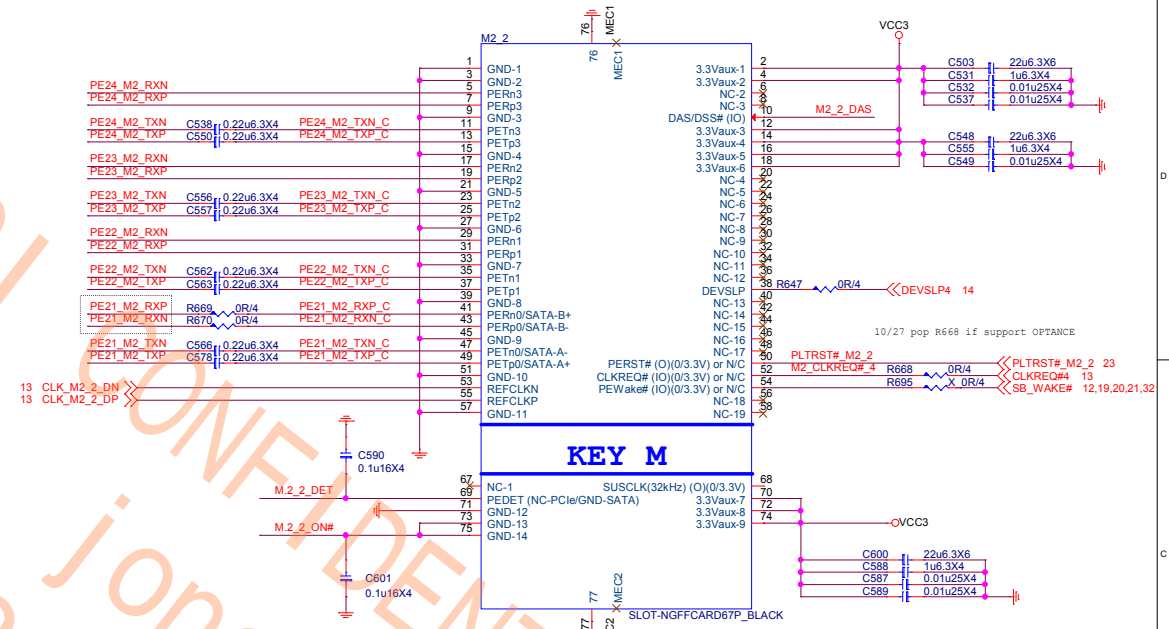
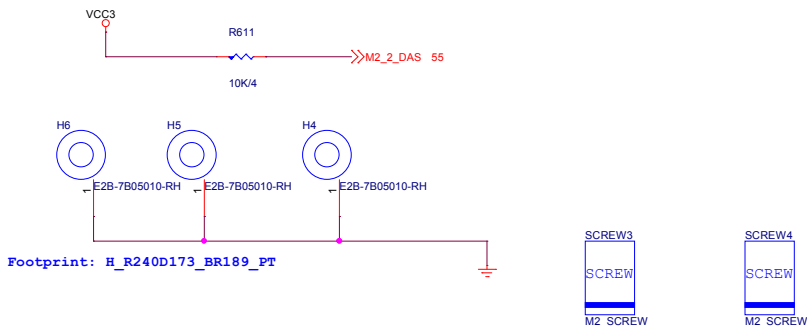
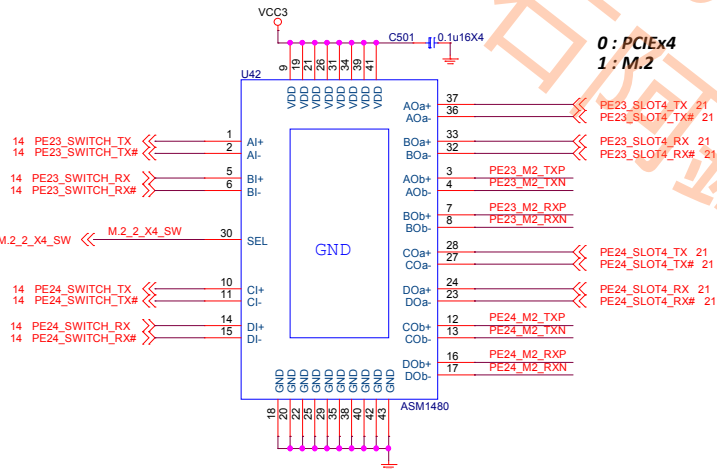
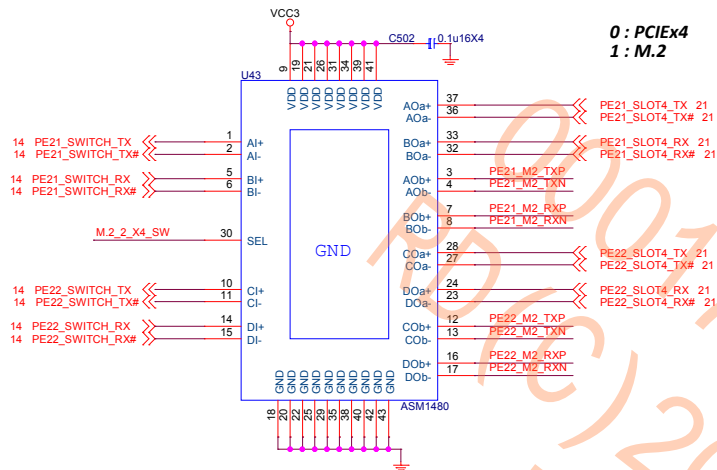


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BIOS_MODE

BIOS_DIS_SW2	M2_2_SEL	Mode
0	0	M2 SLOT-PCIe
0	1	X4 SLOT-PCIe
GPI	GPI	GPI

MICRO-STAR INT'L CO.,LTD

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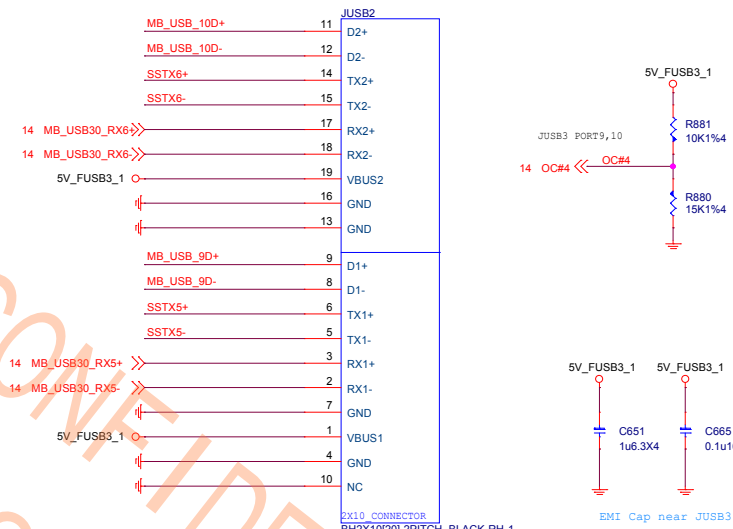
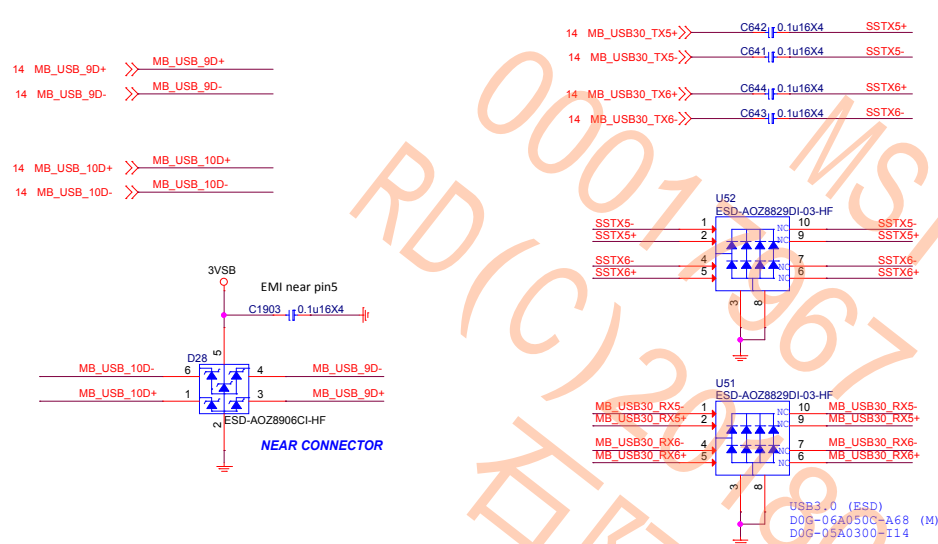
Size: Custom

Document Description: **M.2-SLOT2**

Date: Wednesday, January 03, 2018

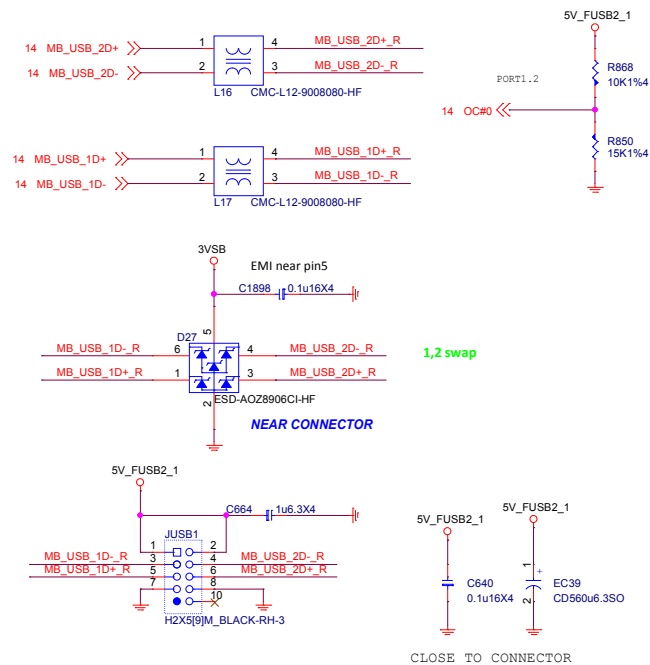
Rev: 1.0

JUSB3 PORT9,10



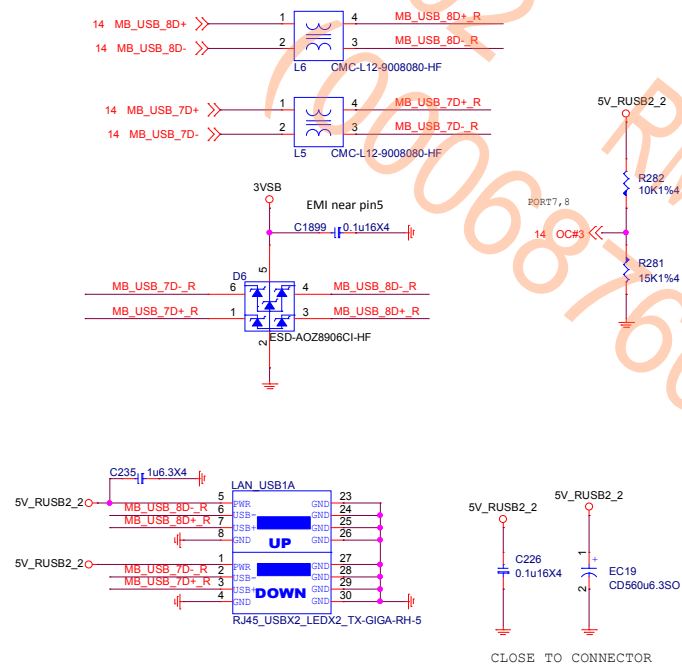
JUSB1 PORT 7,8

2017.12.12
swap 1,2 to 7,8 for layout

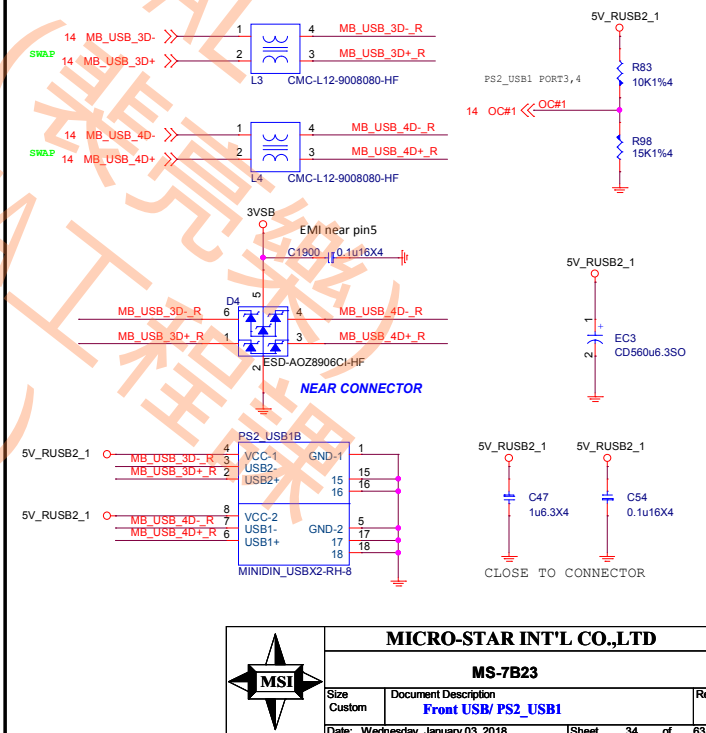


LAN_USB1 PORT 1,2

2017.12.12
swap 1,2 to 7,8 for layout



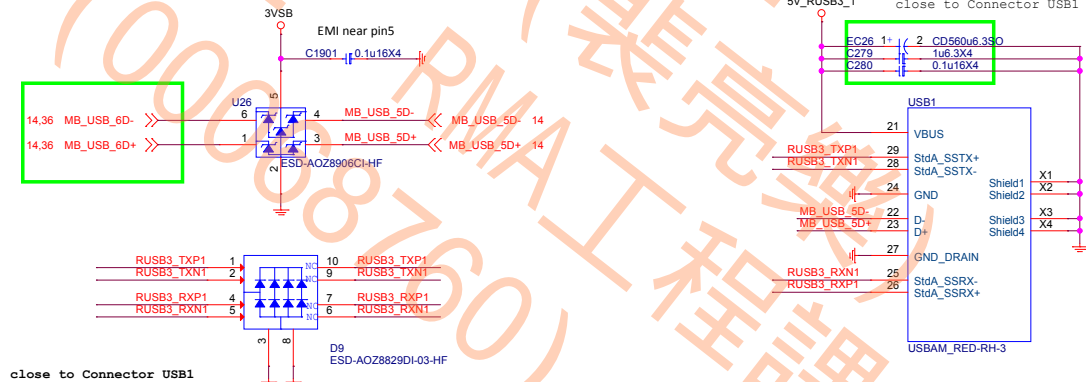
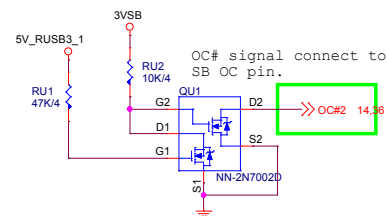
REAR PS2_USB1 PORT 3,4



MICRO-STAR INT'L CO.,LTD

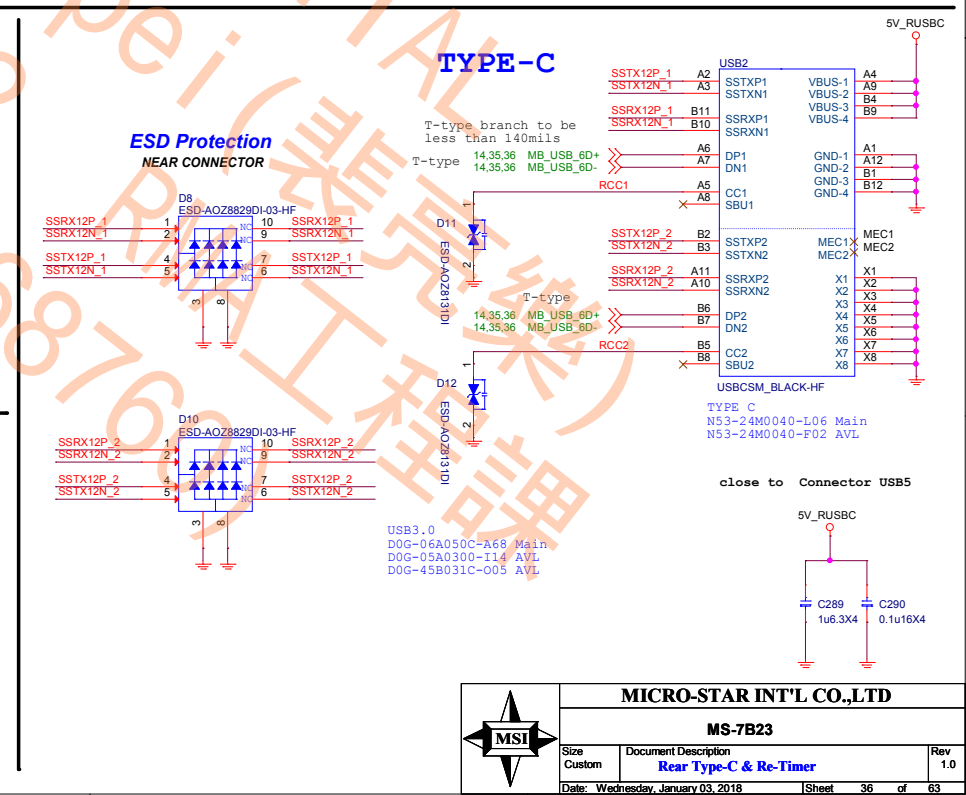
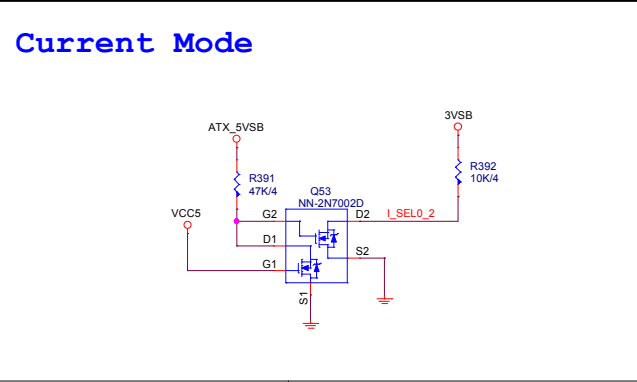
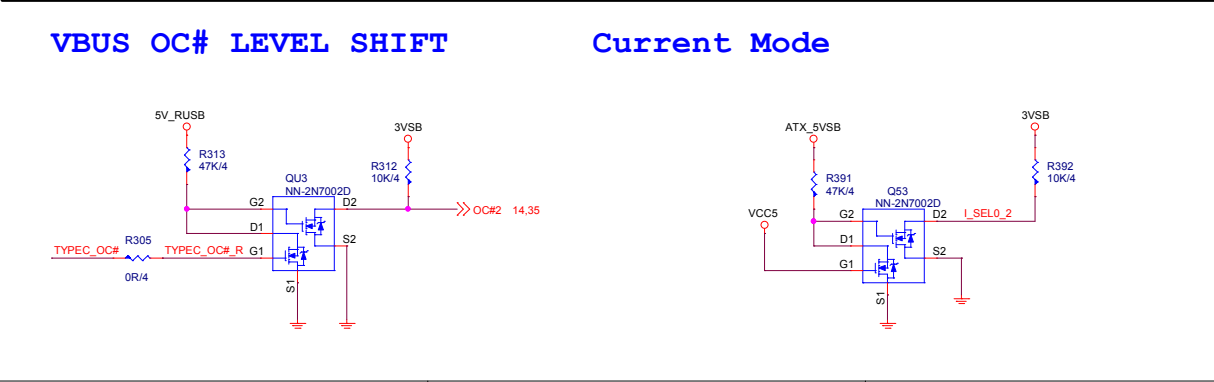
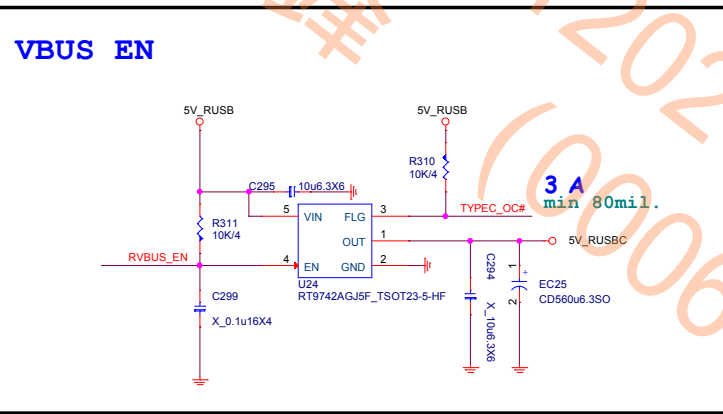
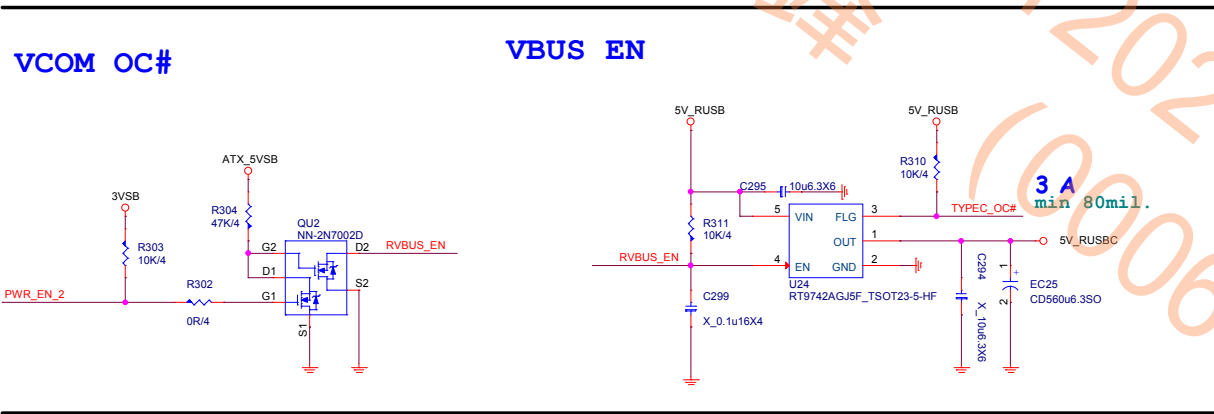
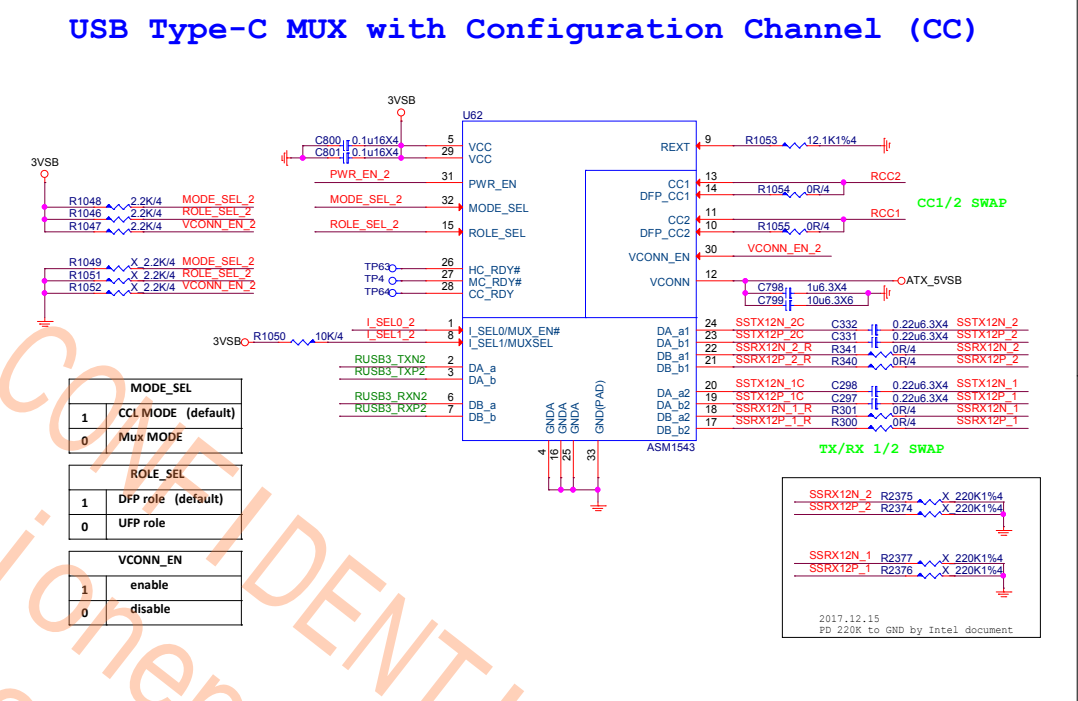
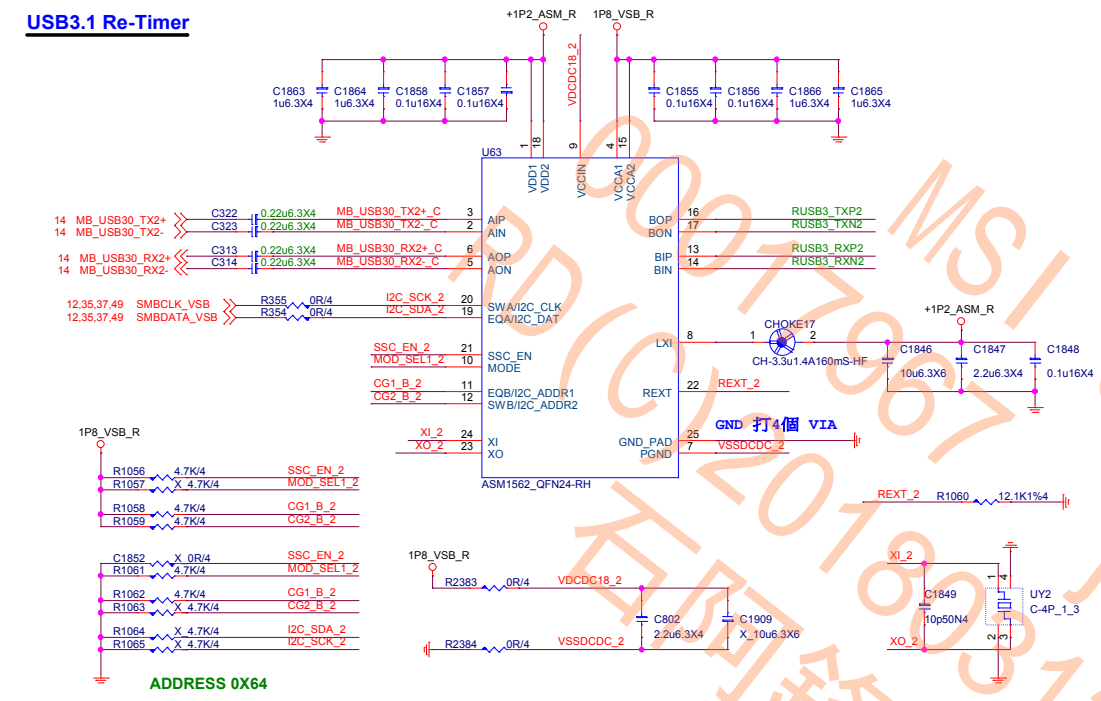
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Size Custom	Document Description Front USB/ PS2_USB1	Rev 1.0
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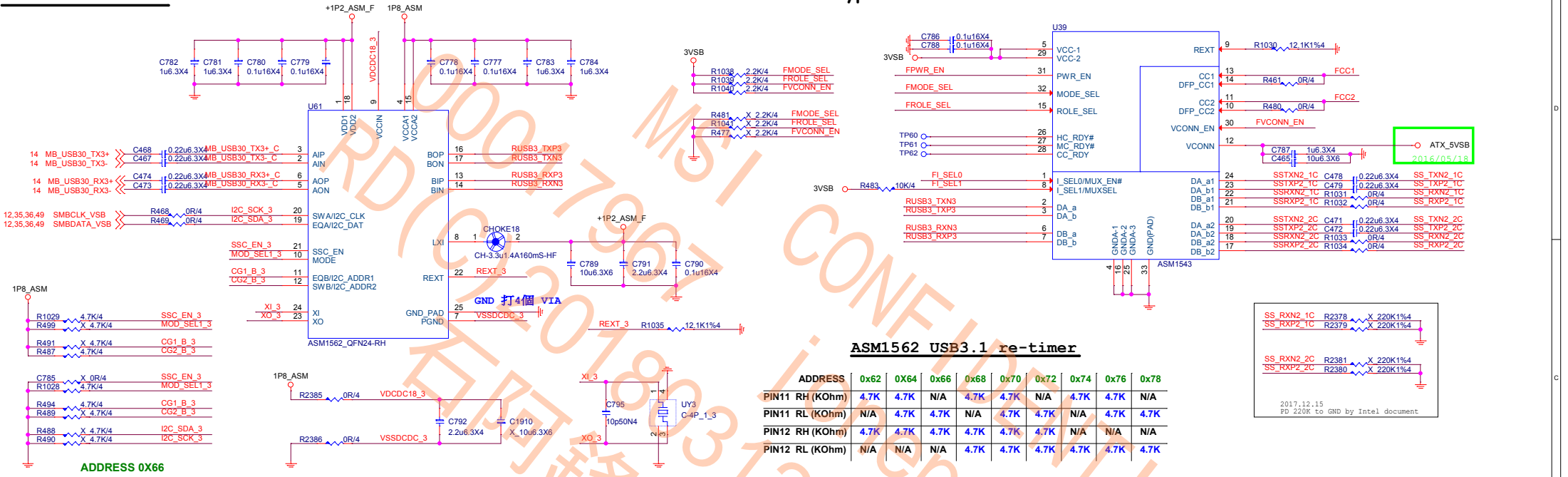
Size Custom	Document Description Type-A & Re_driver	Rev 1.0
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USB3.1 Gen2 Re-Timer

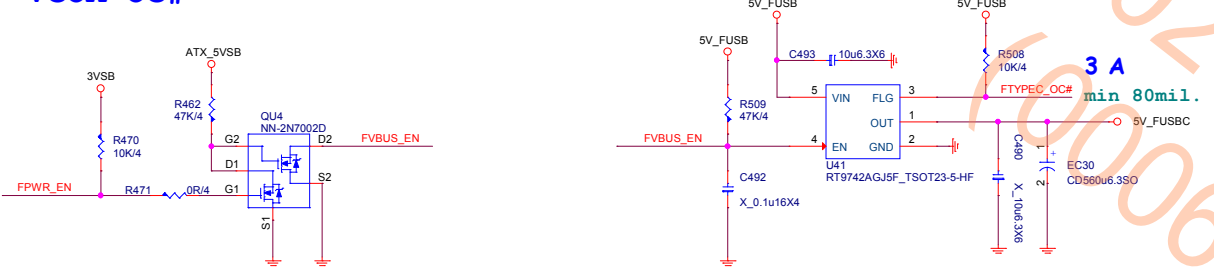
USB Type-C MUX with Configuration Channel (CC)

USB 3.1-Type-C



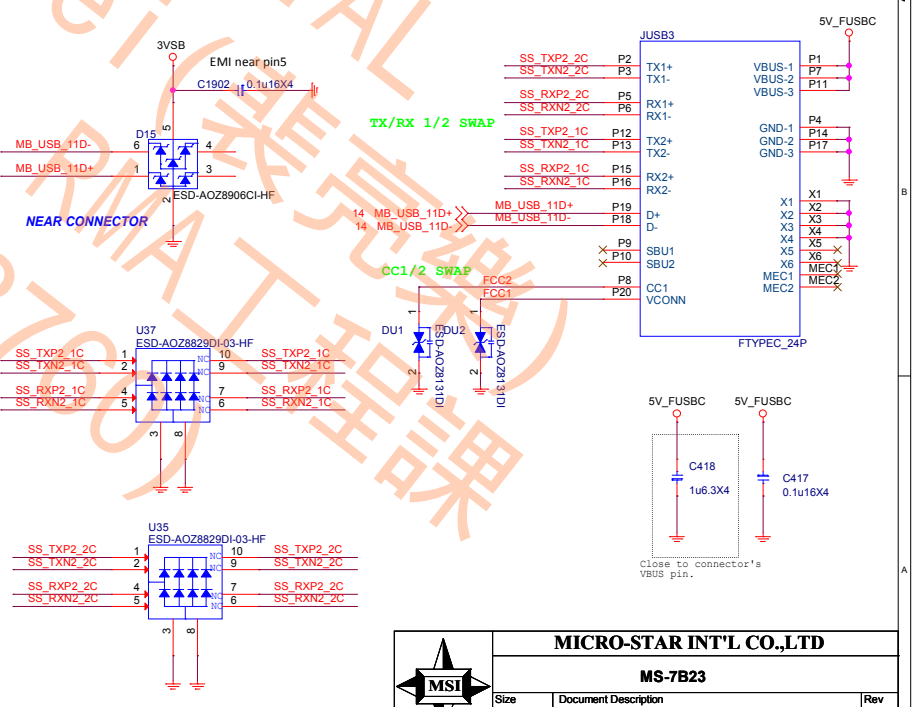
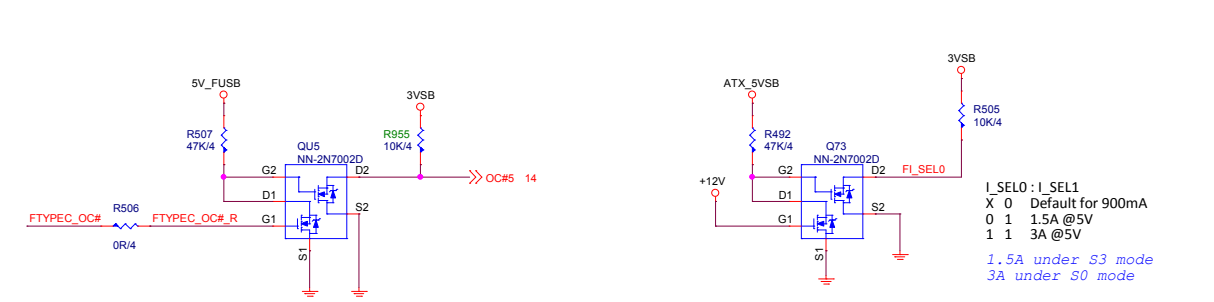
VCOM OC#

VBUS EN

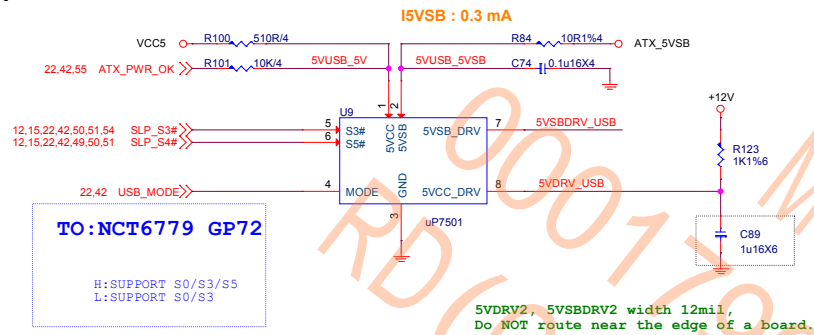


VBUS OC# LEVEL SHIFT

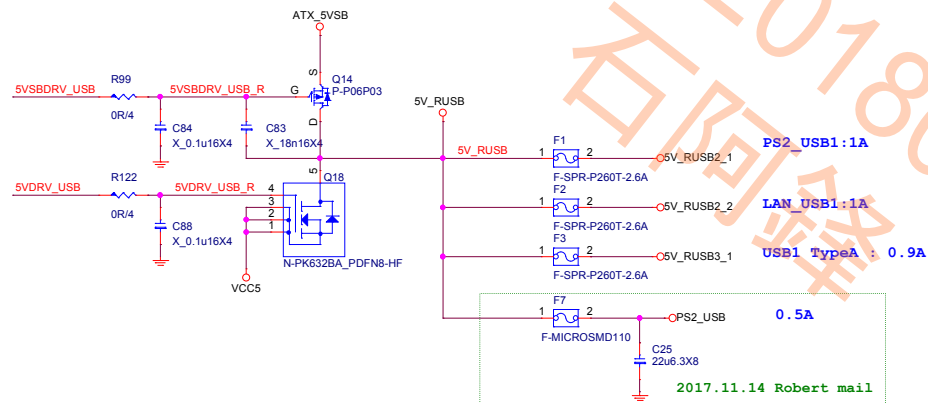
Current Mode



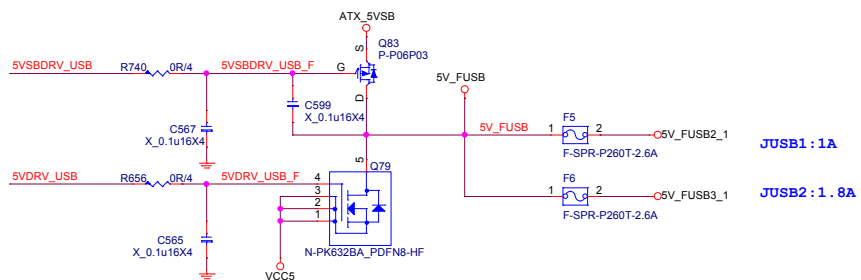
USB POWER



REAR USB PORT POWER

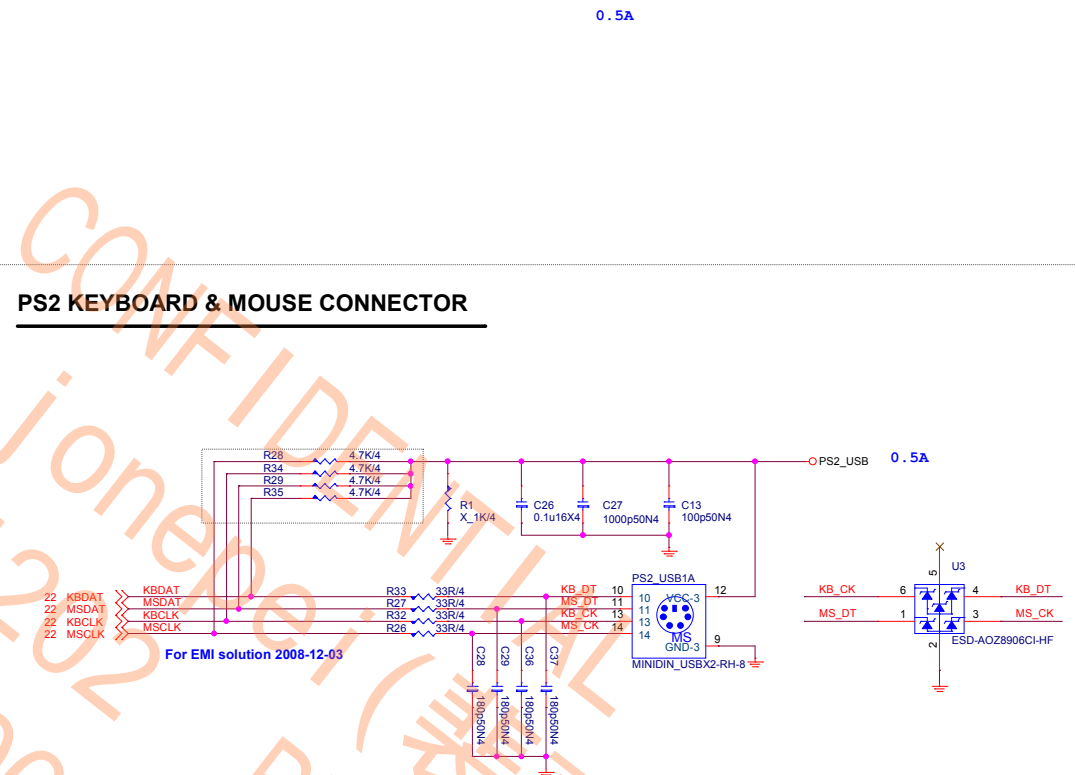


FRONT USB PORT POWER



PS2 POWER

USB MODE



USB_CONN	USB_POWER	PCH_PORT	OC# SIGNAL
LAN_USB1	5V_FUSB2_1	Port5,6	OC#0
FS2_USB1	5V_RUSB2_2	Port9,10	OC#1
USB1	5V_FUSB3_1	Port1,2	OC#2
JUSB3	5V_RUSB3_1	Port3,4	OC#3
JUSB2	5V_RUSB2_1	Port7,8	OC#4



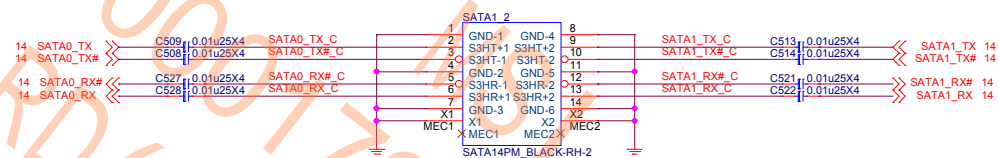
MICRO-STAR INT'L CO.,LTD

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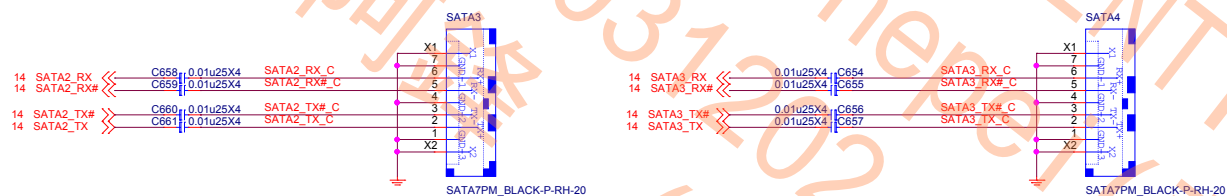
SATA PORT 0,1

Black 90 degree



SATA PORT 2,3

Black 180 degree



MICRO-STAR INT'L CO.,LTD

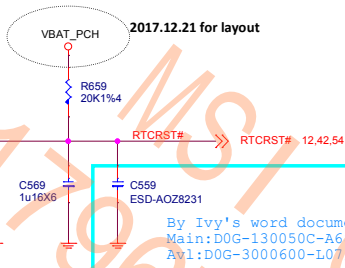
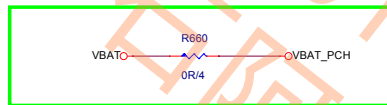
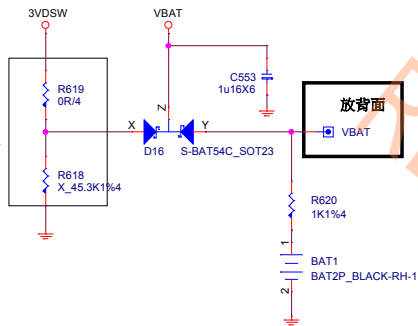
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Custom	SATA connector	1.0
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VBAT

Cut VBAT

follow CRB
2017.12.21
Robert mail



Function 1		
IN		OUT
INPUT1	INPUT2	OUTPUT1
0	1	1
1	0	0
1	1	0
0	0	0

Default

Function 2				
IN		OUT		
INPUT3 & lowswitch EN	INPUT4	OUTPUT2	OUTPUT3	VOUT
0	0	0	1	1
1	0	1	1	0 (discharge)
0	1	1	0	0 (discharge)
1	1	1	0	0 (discharge)

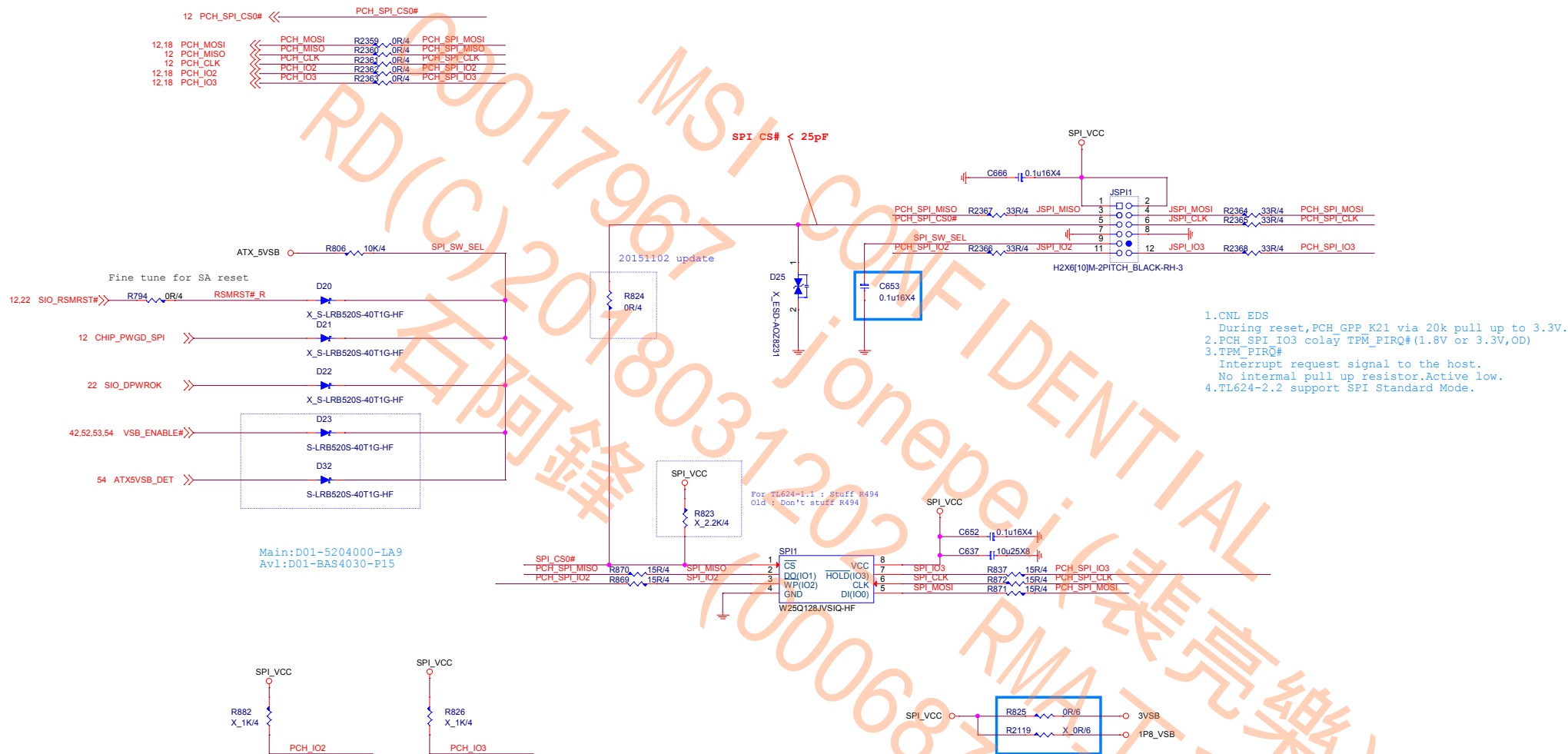
Default



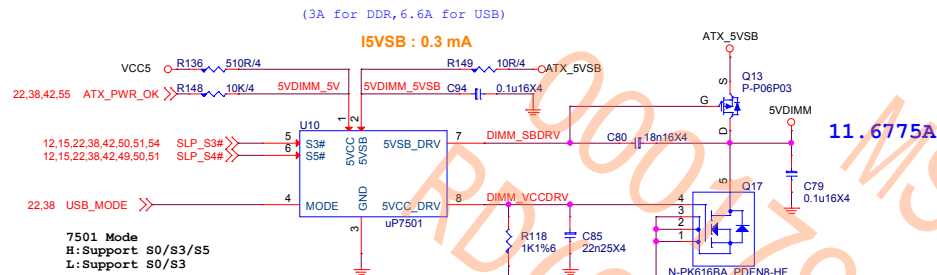
MICRO-STAR INT'L CO.,LTD

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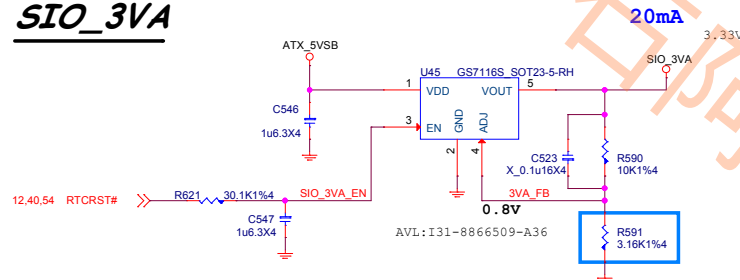
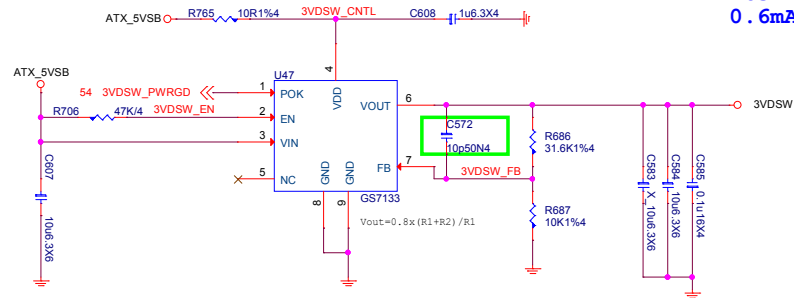
Size	Document Description	Rev
Custom	CUT VBAT circuit	1.0
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5VDIMM FOR DDR



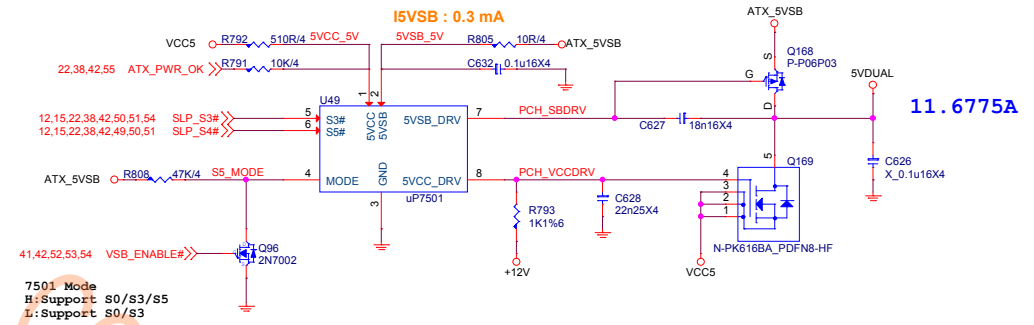
SIO_3VA

3VDSW

113mA (PCH)
165mA (I219)
0.6mA (RTC)

5VDUAL

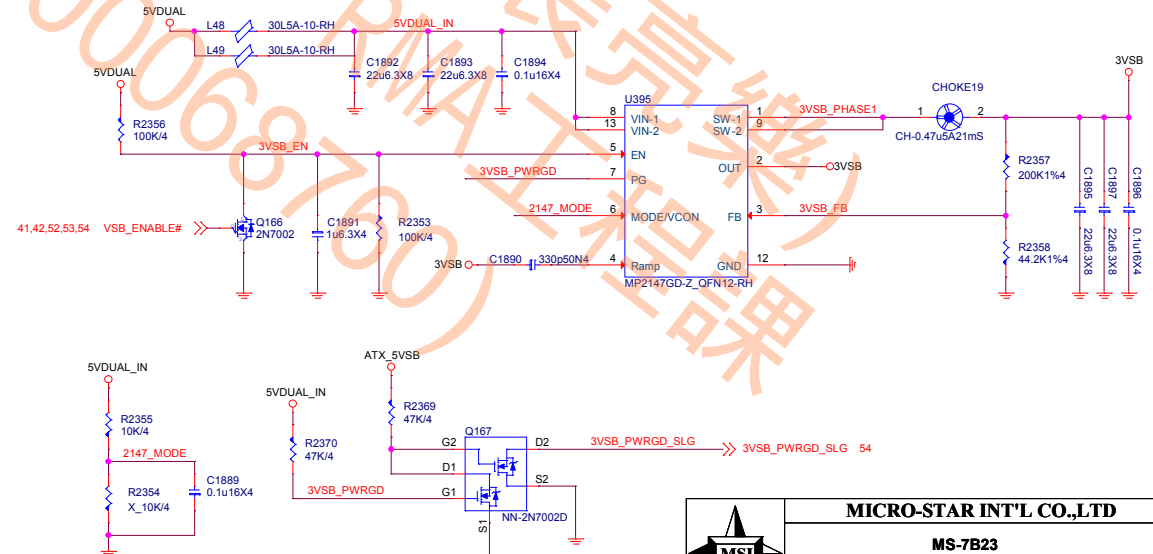
5VDUAL is power source of 1P0SB, 1.8PSB & 3VSB



11.6775A

For power 700W solution (only for uP7501+uP7506 for 3V5B solution)
The power supply VCC3 delay 12ms after VCC5 assert.
The chip u7501 5VDRV1 work when the VCC5 ready
(When VCC5 up to 4.2V and the 5VDRV1 delay 6ms assert), but
VCC3 not ready and let the 3V5B sequence fail.

3VSB



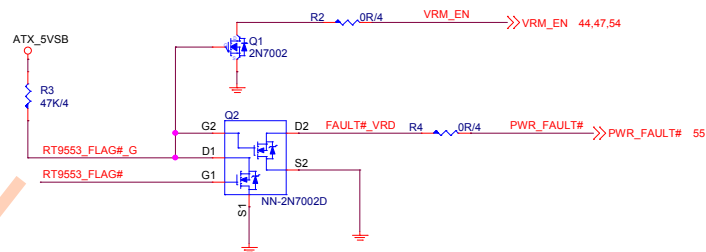
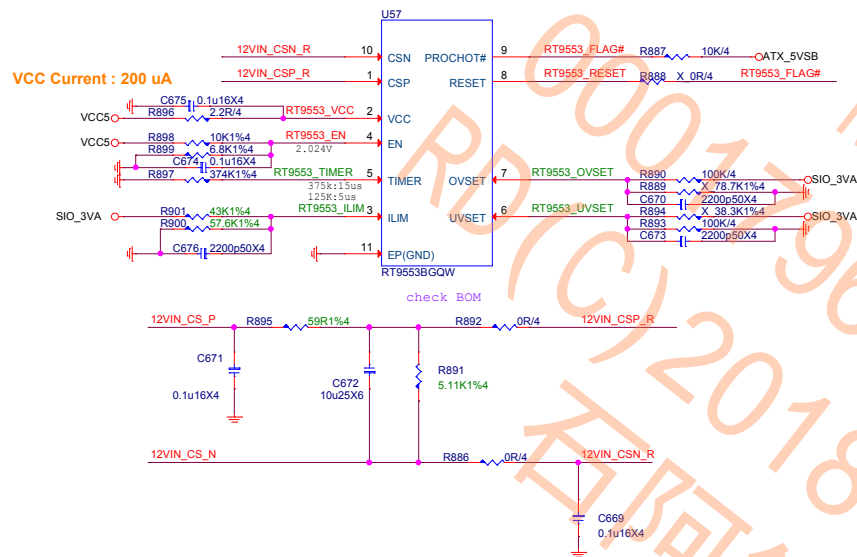
3.889A



MICRO-STAR INT'L CO.,LTD

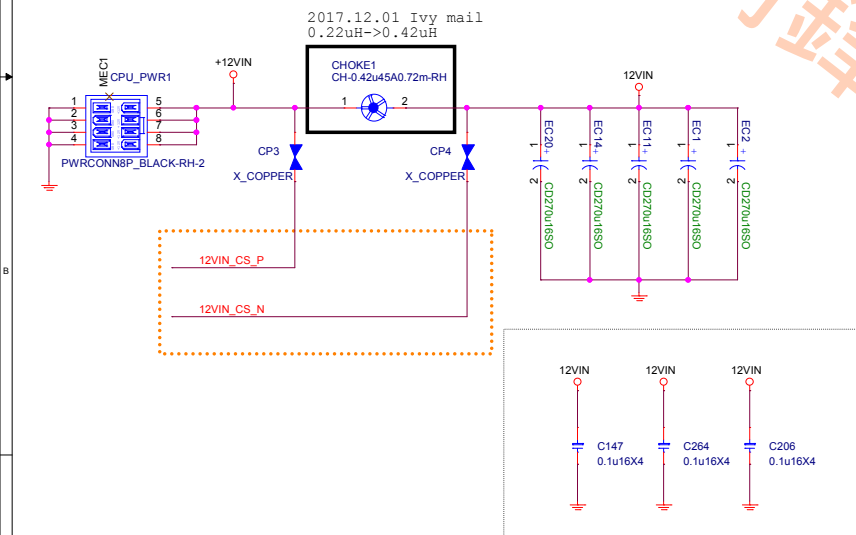
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OCP: 30A
Real OCP: 30.05A
R17+R18>100k V_{sio_3va}= 3.38V R_{dcr}= 0.5 mohm

$I_{3933_imon} * [R17 * R18 / (R17 + R18)] = I_{step} * R_{dcr} * 100$
 $I_{3933_imon} = 10 \mu A / step$
 $I_{step} = 4.968A$



D=Vout/Vin		
Vin = 12	> input voltage	
Vout = 1.52	> output Vcore	
D = 0.126667		

Io = Icore(max)*0.8		
I core(max) = 138	> Vcore current	
I avg. = 110.4	A	

I ripple={ Io*√D*√(1-D) } / Phase		
Phase = 4	phase	
I ripple = 9.179738	A	

How many pcs. Of Cap.		
I ripple(cap) = 5000	m A	
COE _{TEMP} = 1		
Input Cap. = 2	pcs.	

CORE:
D = Vout/Vin
= 1.52/12
= 0.126667
N = 4
I_{rms} = I_{out} * [D/N - (D)^2]^(1/2)
= 138 * (0.031667 - 0.016044)^(1/2)
= 17.2489A

D=Vout/Vin		
Vin = 12	> input voltage	
Vout = 1.52	> output Vcore	
D = 0.126667		

Io = Icore(max)*0.8		
I core(max) = 45	> Vcore current	
I avg. = 36	A	

I ripple={ Io*√D*√(1-D) } / Phase		
Phase = 2	phase	
I ripple = 5.986785	A	

How many pcs. Of Cap.		
I ripple(cap) = 5000	m A	
COE _{TEMP} = 1		
Input Cap. = 2	pcs.	

GT:
D = Vout/Vin
= 1.52/12
= 0.126667
N = 2
I_{rms} = I_{out} * [D/N - (D)^2]^(1/2)
= 45 * (0.063333 - 0.016044)^(1/2)
= 9.7857A

D=Vout/Vin		
Vin = 12	> input voltage	
Vout = 0.95	> output Vcore	
D = 0.079167		

Io = Icore(max)*0.8		
I core(max) = 6.4	> Vcore current	
I avg. = 5.12	A	

I ripple={ Io*√D*√(1-D) } / Phase		
Phase = 1	phase	
I ripple = 1.382393	A	

How many pcs. Of Cap.		
I ripple(cap) = 5000	m A	
COE _{TEMP} = 1		
Input Cap. = 1	pcs.	

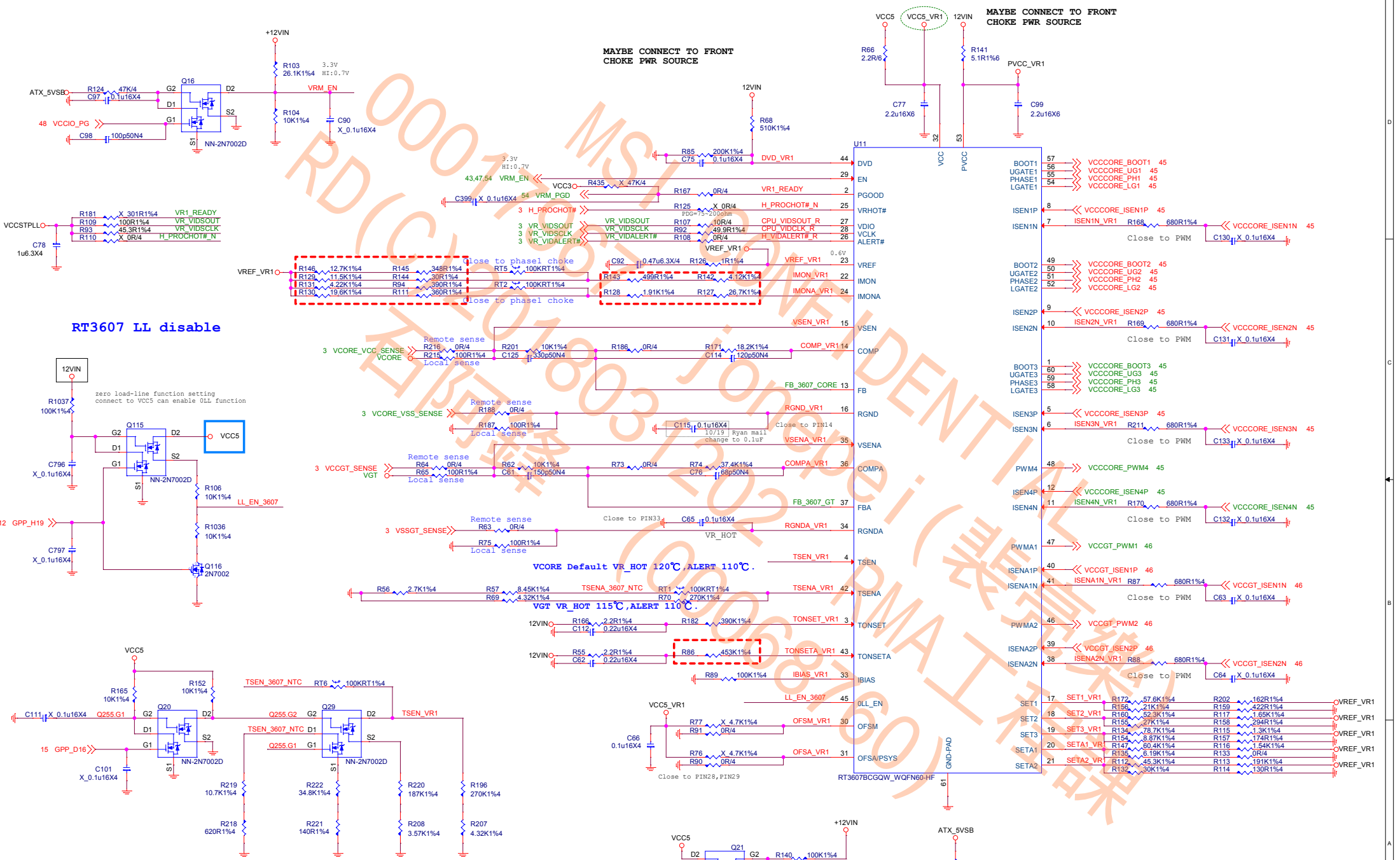
VCCIO:
D = Vout/Vin
= 0.95/12
= 0.079167
N = 1
I_{rms} = I_{out} * [D/N - (D)^2]^(1/2)
= 6.4 * (0.079167 - 0.006267)^(1/2)
= 1.728A



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VCCORE Thermal Protection Table

GPP_D16	R1	R2	Thermal Alert#	VR_HOT#	Thermal Alert# / VR_HOT#
GPI (1) Default	190.57K	11.32K	97°C	115°C	84.35%
GPI (0)	274.32K	34.94K	106°C	115°C	92.17%



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EMI cap for display



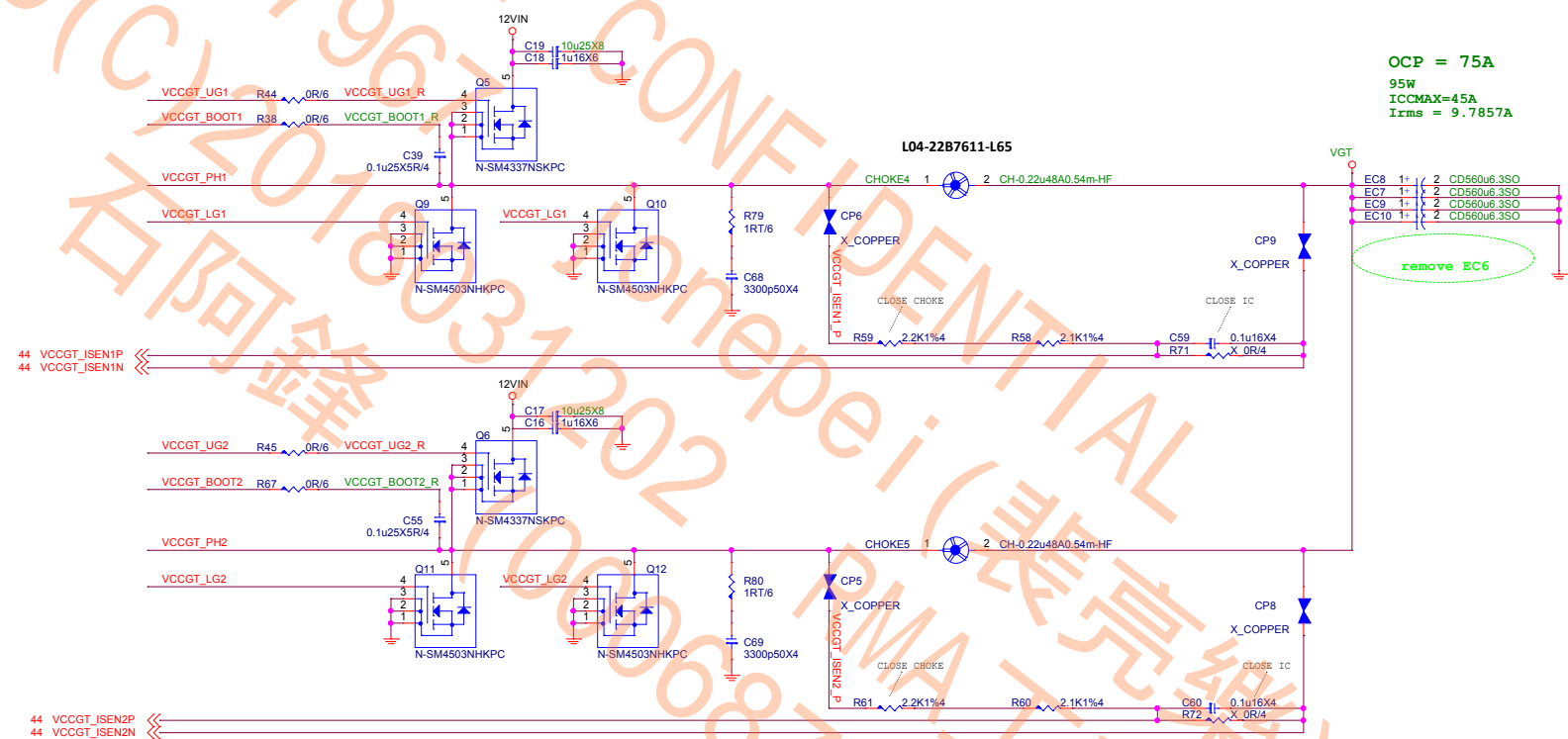
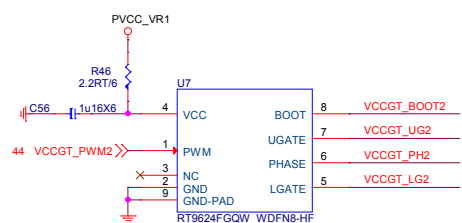
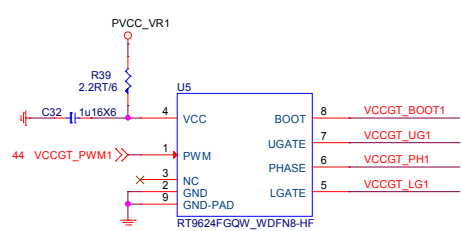
CHOKES:
L04-22B7611-L65

Current limit = 200A
OCP = 200A
95W
ICCMAX=138A
I_{rms} = 17.2489A

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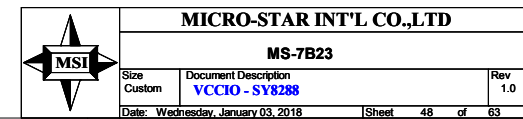
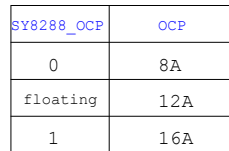
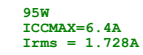
MS-7B23

Size	Document Description	Rev
Custom	VCORE(P-PAK) PHASE1-4	1.0
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OCP = 75A
95W
ICCMAX=45A
Irms = 9.7857A

IMAX 10A
ILIMIT=10A~12A
IOC=ILIMIT+40%*IMAX/2=12A~14A.



DDR4 Power:1.2V,19.8A OCP:28A

3.3A FOR CPU

15.7A FOR 4DIMM

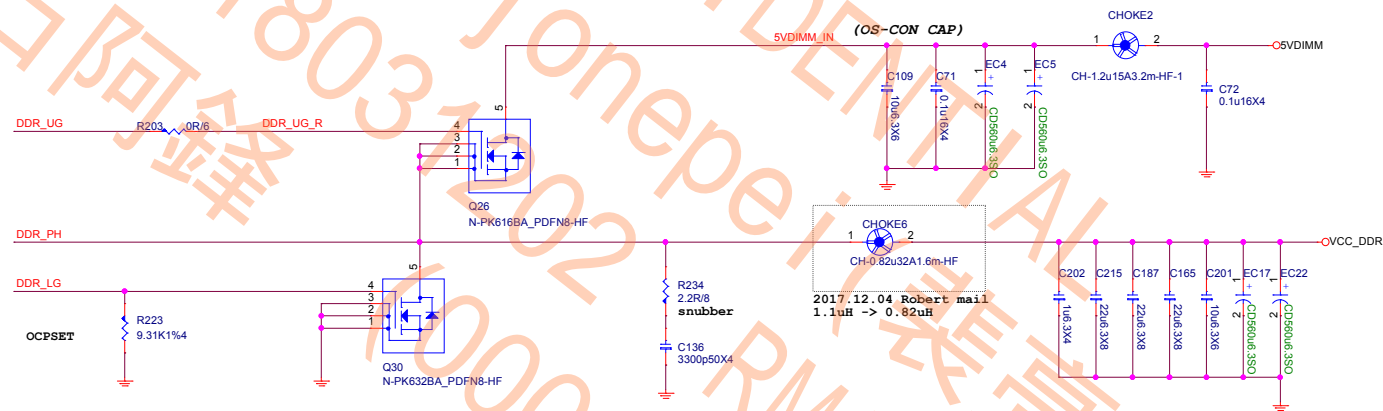
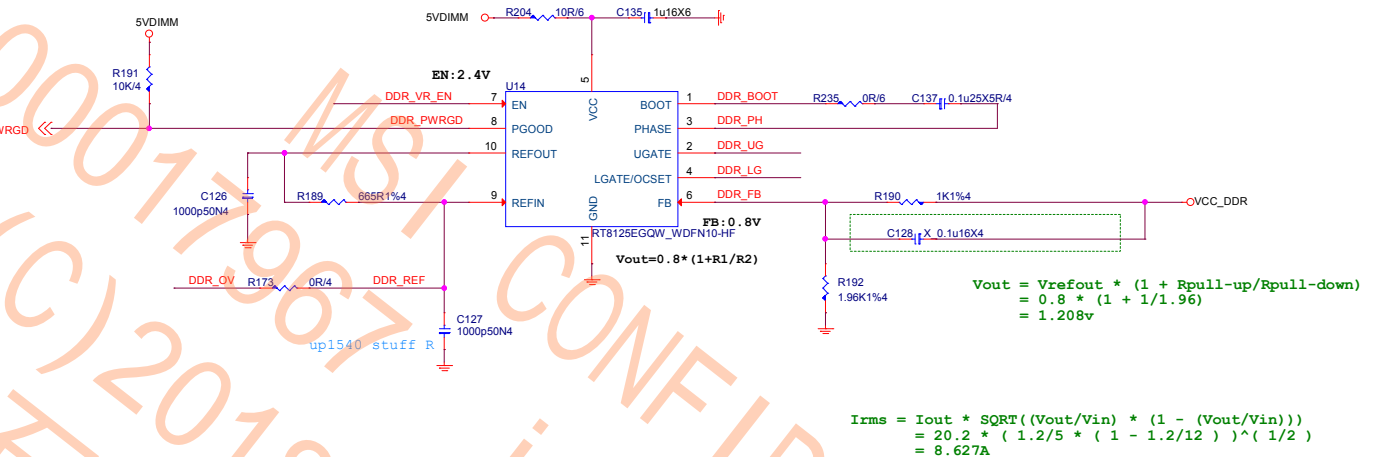
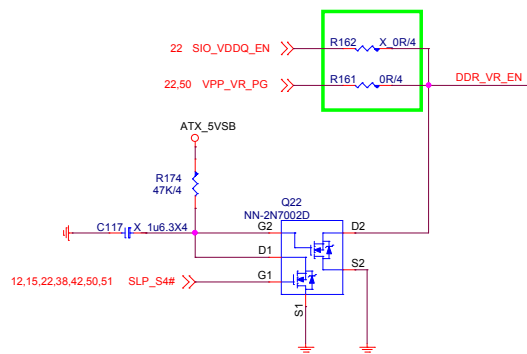
0.7A FOR DDR VTT

OCP = 19.6A

$R_{ocset} = 1.5 * I_{max} * R_{ds(on)} / I_{ocset}$
 $= 28 * 5.1m\Omega / 10uA$
 $= 14.28K$

R_{ds(on)} (low)

D03-4503N0C-ST8 : 5.1mohm

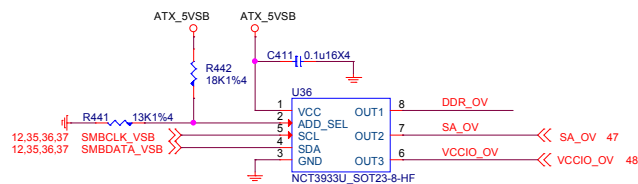


Datasheet公式計算
 $L_{min} = ((V_{in} - 1.2V) / (F_{sw} * k * I_{out_max})) * (V_{out} / V_{in})$
 $= 0.7677uH$ (K = 30%)

若帶入CAP ESR計算, 0.2432uH < L < 1.2897uH

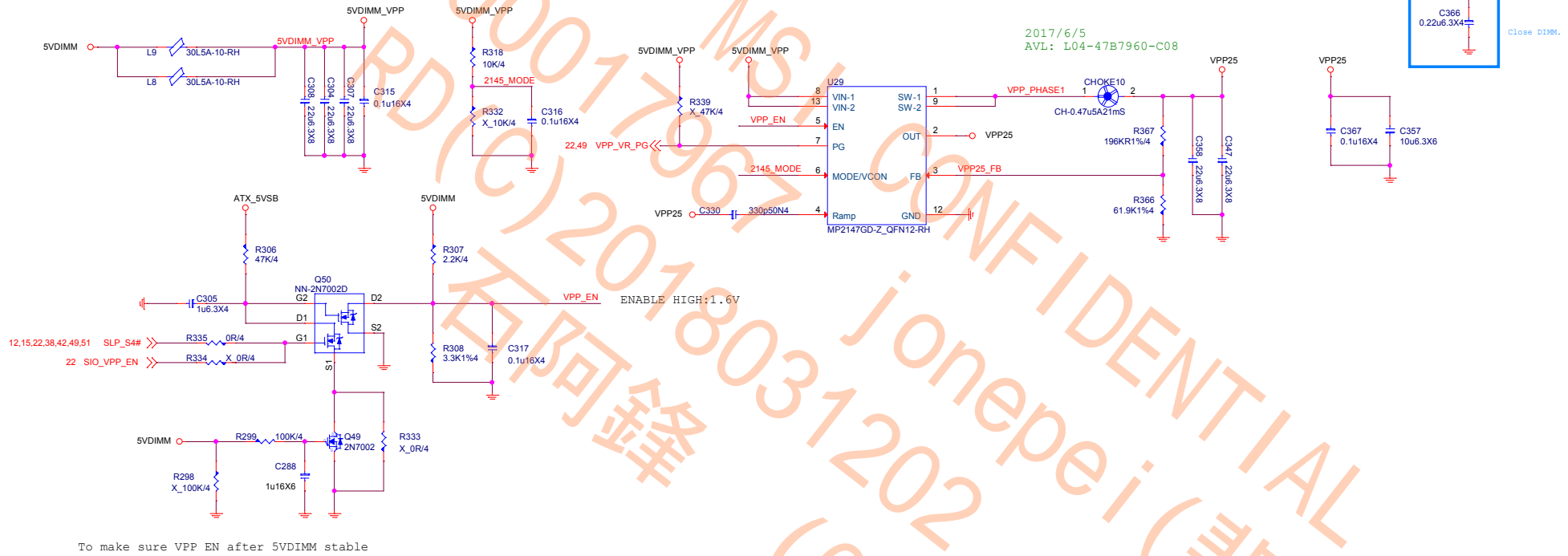
UPI VOLTAGE CONSOLE

0x26: RH=18K, RL=13K



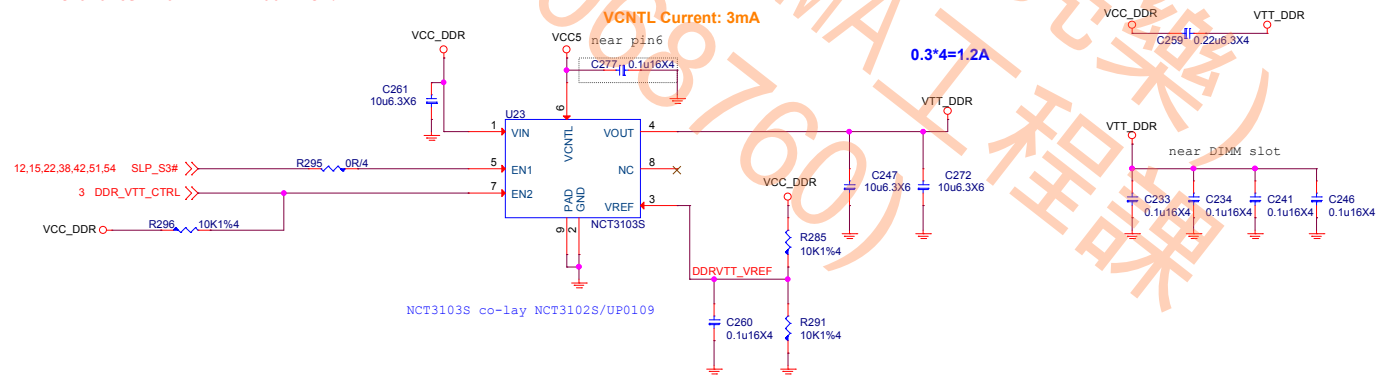
4DIMM :2.24A FOR
DDR VPP2.5V

VPP25 Power
2.5V; 2.24A



DDR VTT Power

To CPU Copper trace width > 250mils , Fill island behind DIMM > 400mils .



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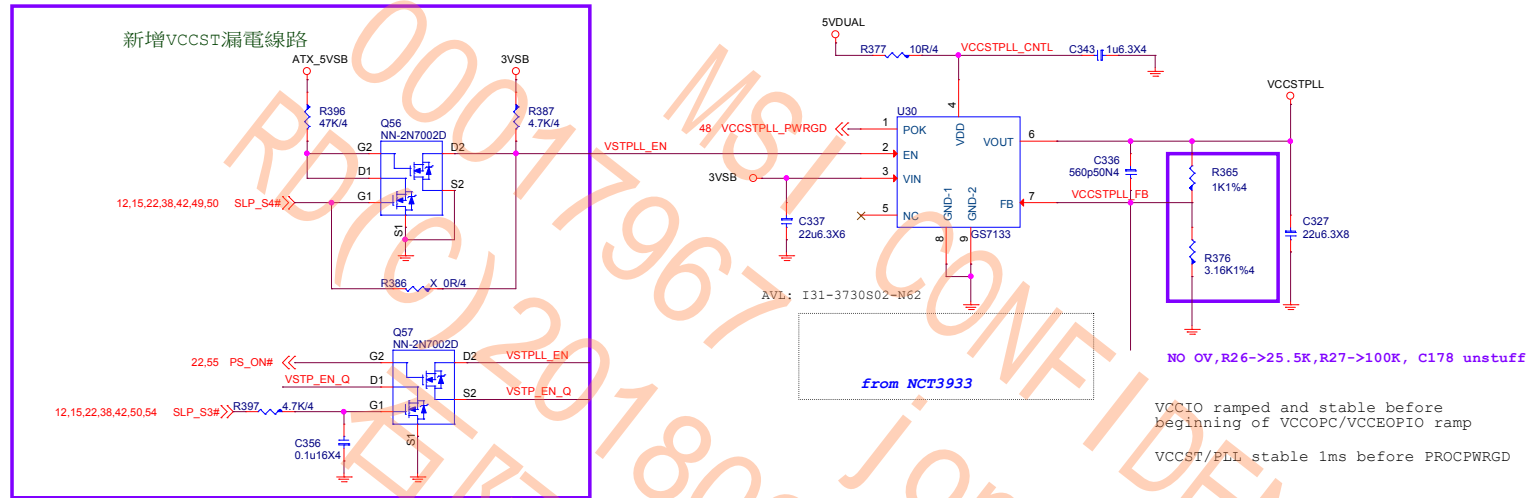
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VCCSTPLL

1.05V; 230mA

For Cost down VCCST&VCCPLL merge



VCCPLL_OC

1.2V; 130mA

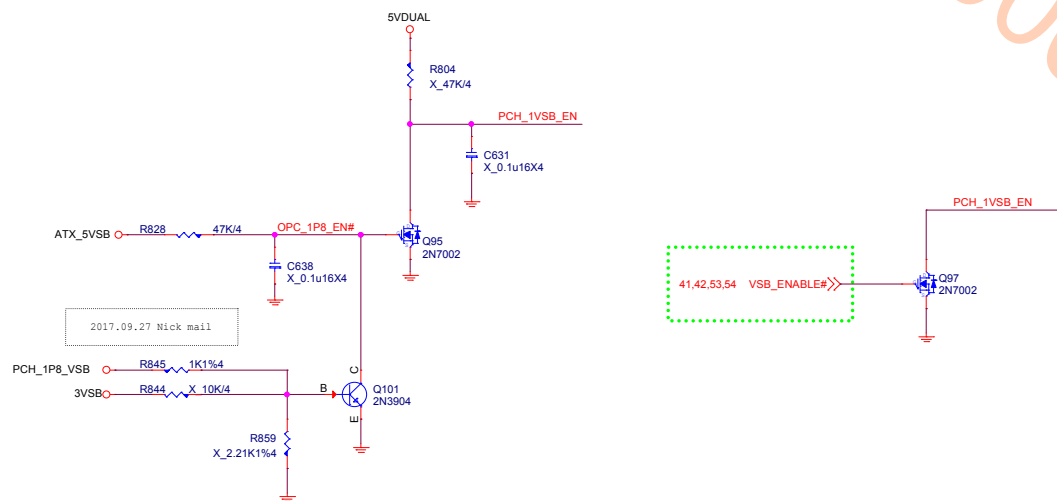
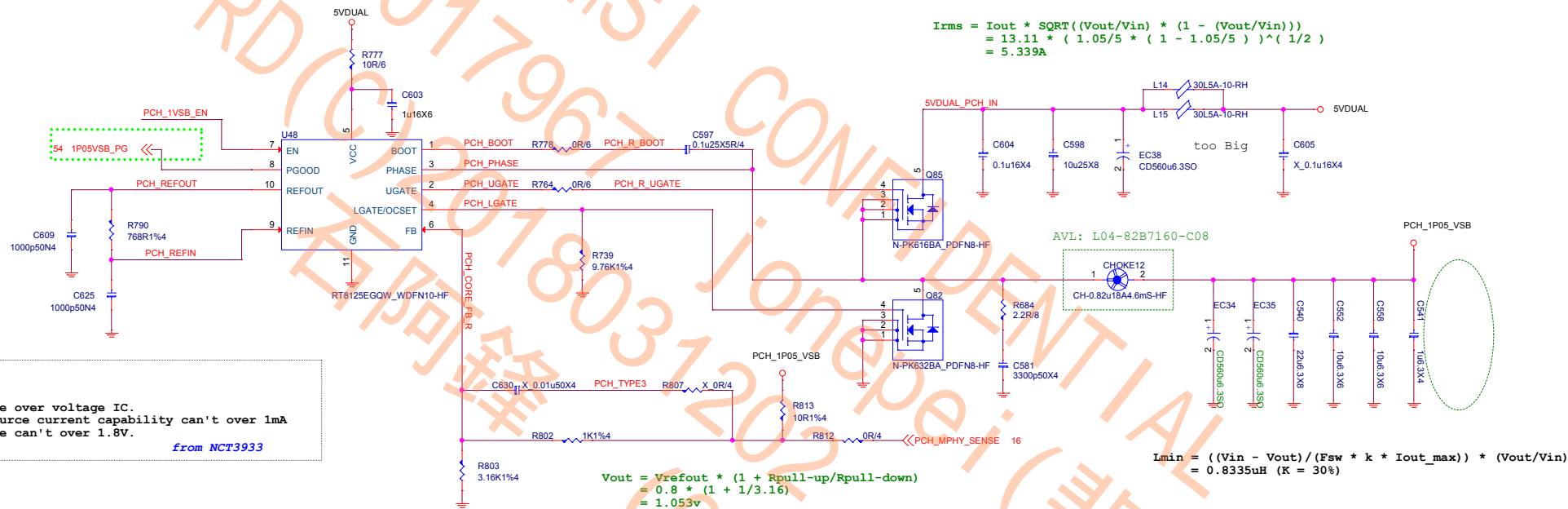
PCH 1VSB

1.05V; 13.11A

$$OCP = R_{ocset} \times I_{ocset} / R_{lqds(on)}$$

$$= 9.76k \times 10u / 4.6m$$

$$= 21.21A$$



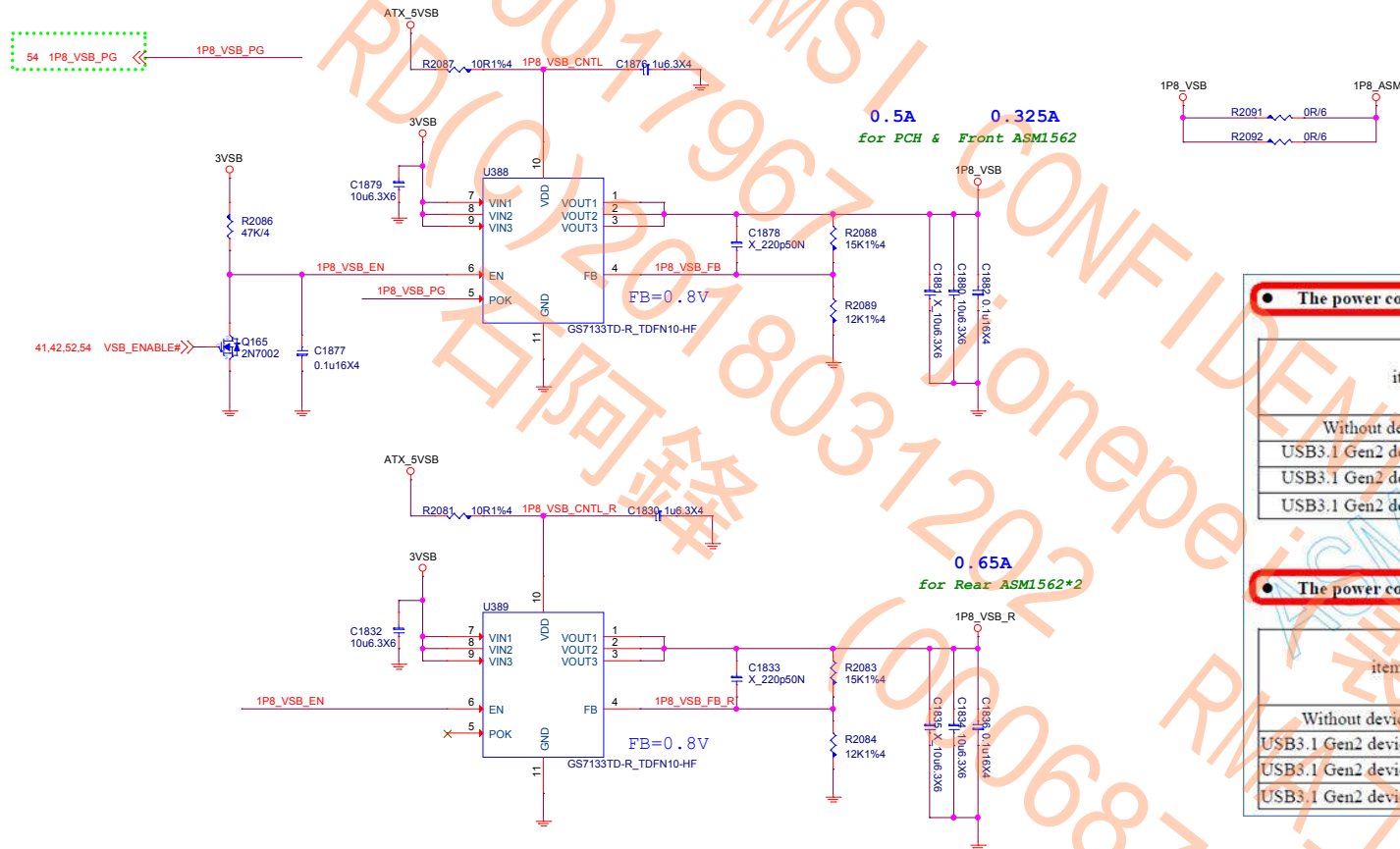
1P8 VSB

1.8V; 500mA

Current Limit: 3.8A

2017.12.07

GS7133 down size to I31-S71330C-N03.



The power consumption with Internal LDO

item	Power state	VCCA 1.8V (mA)	Total power (mW)
Without device plug in.	Power on	25.82	46.47
USB3.1 Gen2 device is plugged in	Burning state	324.60	584.29
USB3.1 Gen2 device is plugged in	In idle	50.58	91.05
USB3.1 Gen2 device is plugged in	S3(D3) state	50.59	91.06

The power consumption with External LDO

item	Power state	VCCA 1.8V (mA)	VDD 1.2V (mA)	Total power (mW)
Without device plug in.	Power on	10.46	17.47	39.79
USB3.1 Gen2 device is plugged in	Burning state	95.34	226.37	443.25
USB3.1 Gen2 device is plugged in	In idle	17.18	52.10	93.44
USB3.1 Gen2 device is plugged in	S3(D3) state	17.17	52.10	93.42



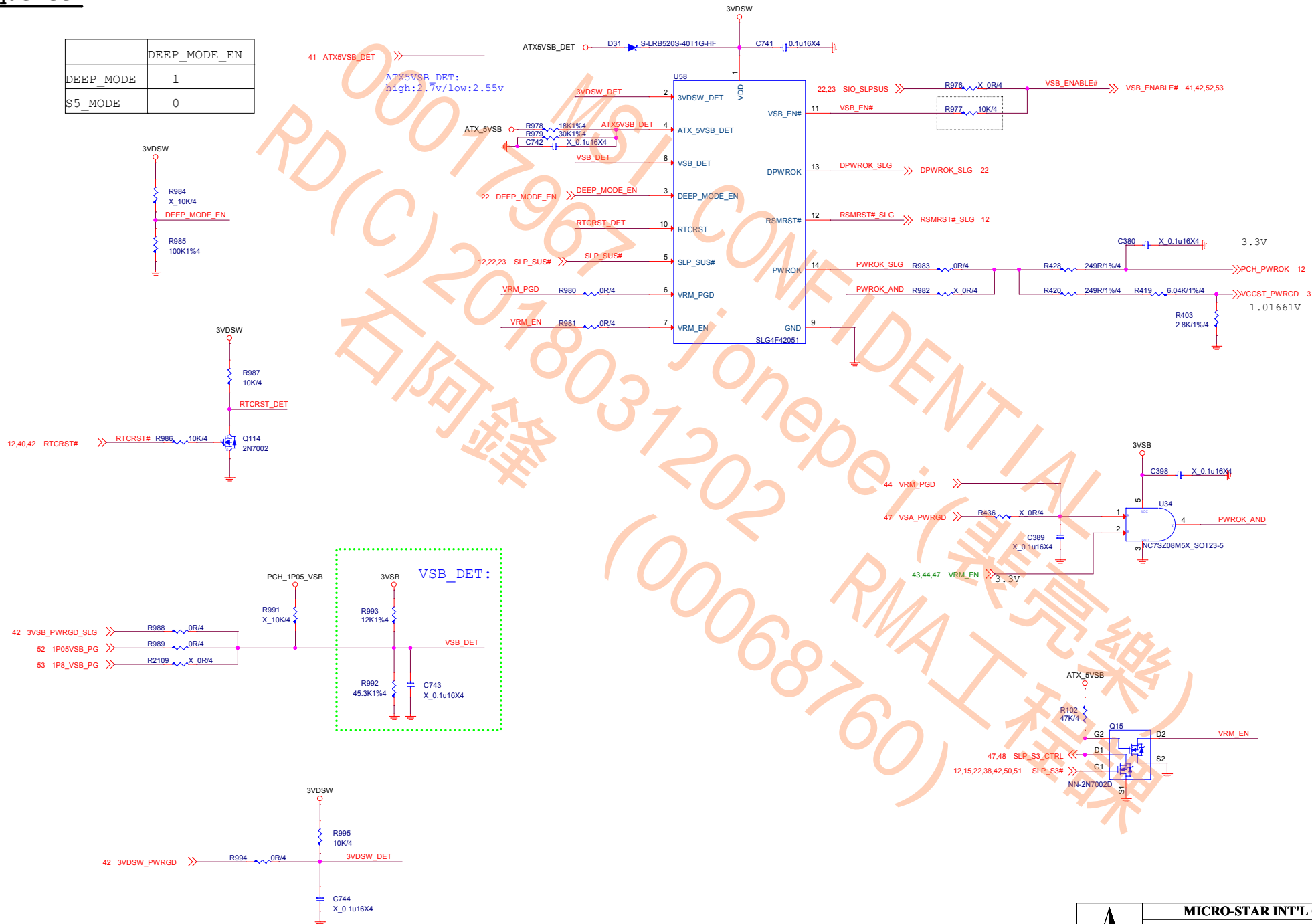
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Custom	PCH 1P8V	1.0
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Sequence

	DEEP_MODE_EN
DEEP_MODE	1
S5_MODE	0



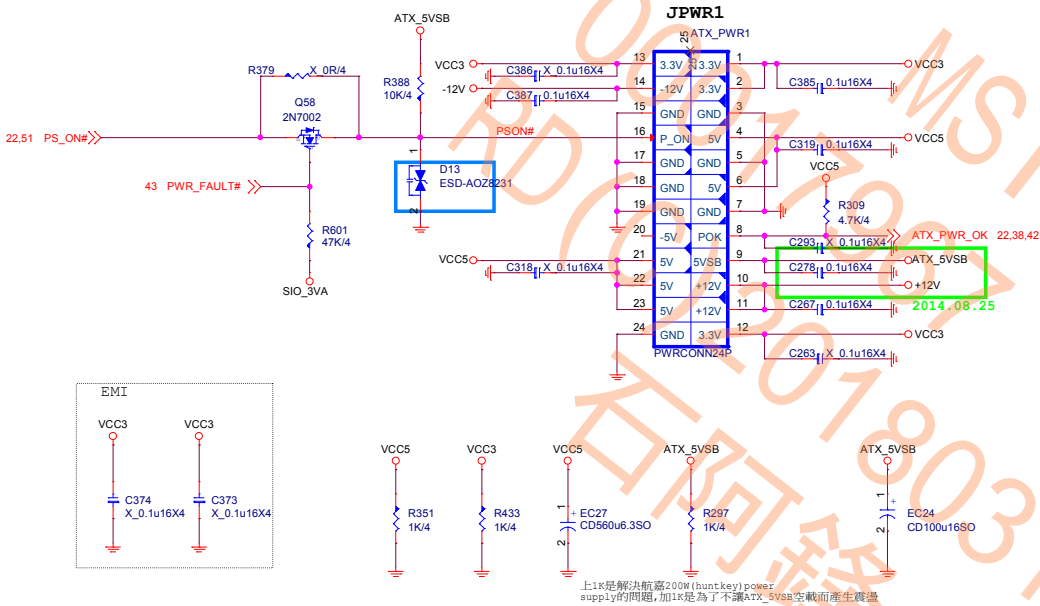
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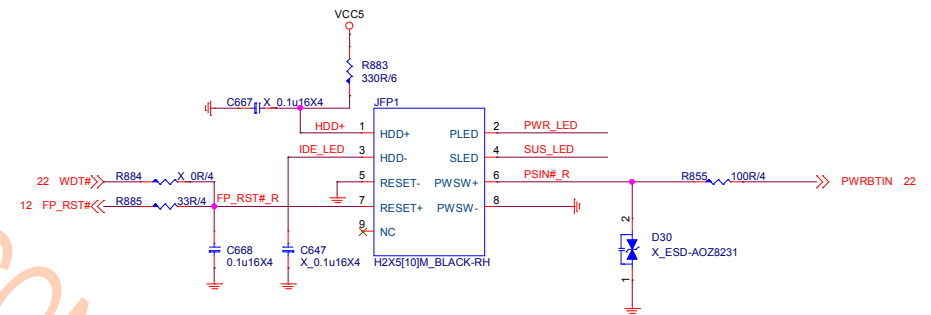
Size Custom	Document Description CPU PWR-VRM-Sequence	Rev 1.0
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ATX POWER CONNECTOR

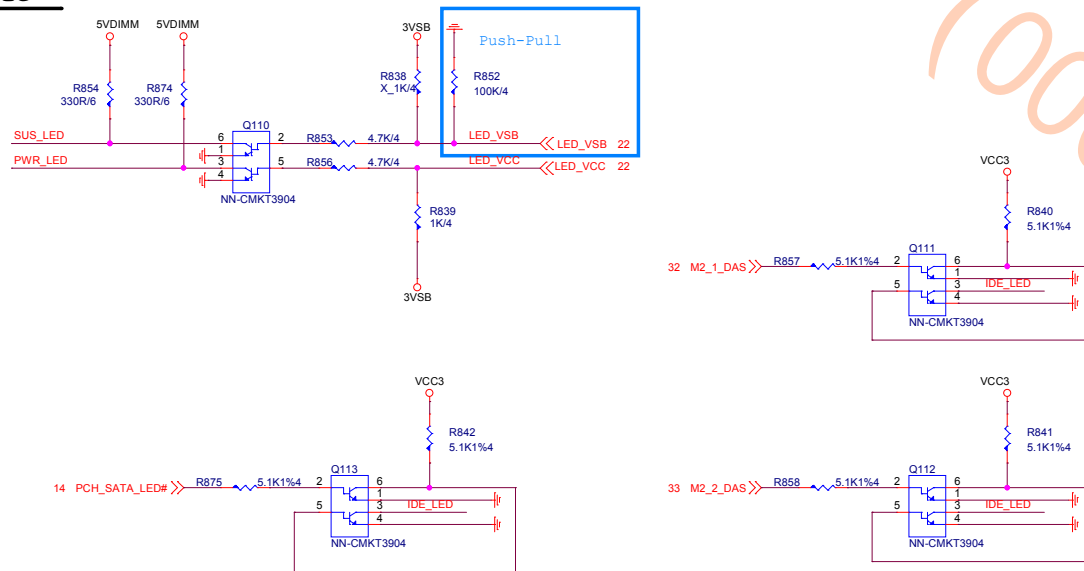
D26:By Ivy's word document.
Main:D0G-130050C-A68
Av1:D0G-3000600-L07/D0G-1200520-I05



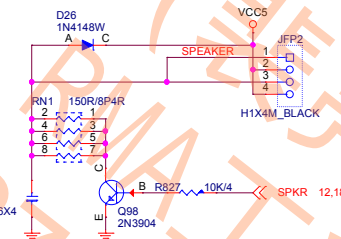
FRONT PANNEL



LED

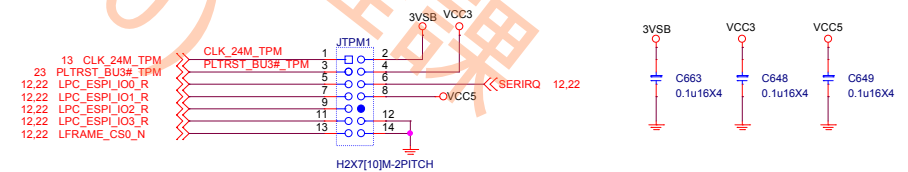


Speaker Pin Header

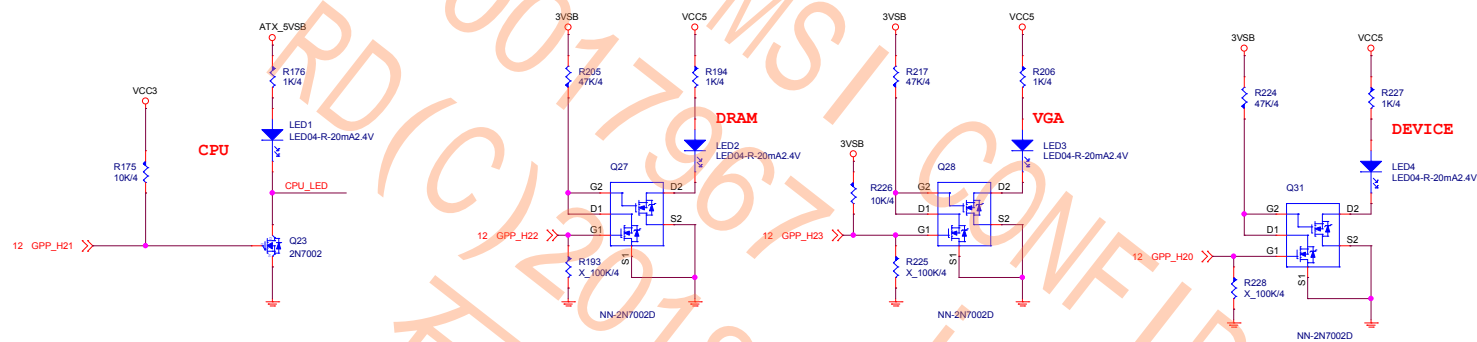


TPM

Don't colay espi debug.



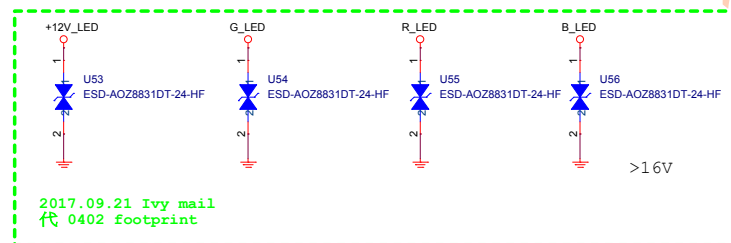
DEBUG LED



GPIO	PCH_GP20	PCH_GP21	PCH_GP22	PCH_GP23
LED				
亮	NATIVE PULL HIGH	GPO PULL HIGH	GPO PULL HIGH	NATIVE PULL HIGH
滅	NATIVE LOW	GPO LOW (default LOW)	GPO LOW (default LOW)	GPO LOW (default LOW)

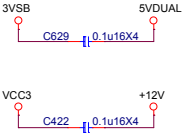
- 關機斷電狀態下，3個LED先維持default全暗，開機通電後：
1. 首先進行CPU checkCPU LED 亮，check PASS後則CPU LED滅掉。
 2. 接著依序進行Memory /memory LED亮check PASS後則memory LED滅掉。
 3. VGA的check/VGA LED亮，check PASS後則VGA LED滅掉。
 4. 因此最後正常順利開機後，三個LED燈都是滅掉的。（系統重啟或其他原因造成系統重開機，則LED仍按上述行為動作）

LED STRIPLINE

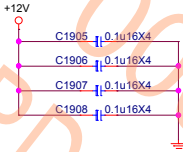


EMI CAP

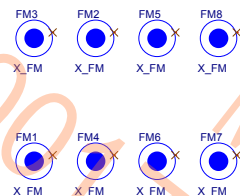
2017.10.13 moat cap



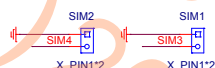
2017.12.21 SA_PH decouple cap



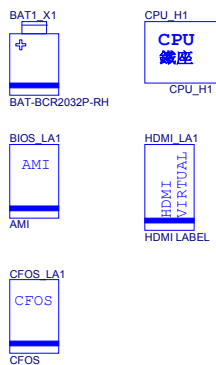
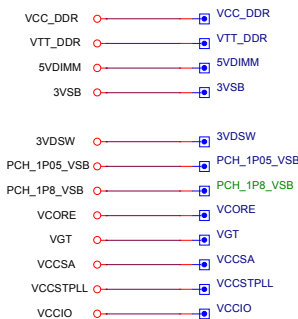
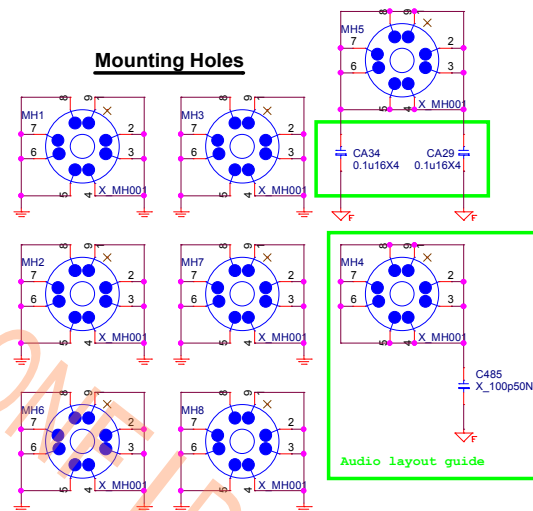
Optical Fiducial Marks-120



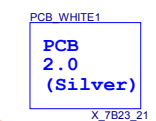
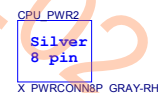
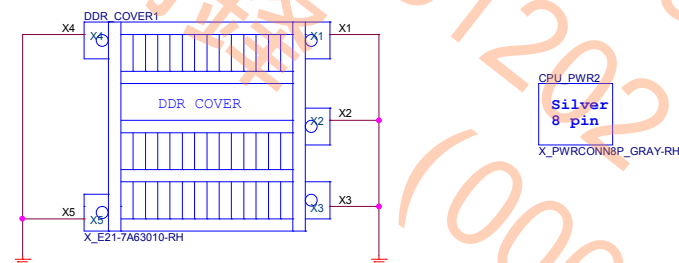
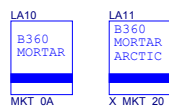
Simulation



Mounting Holes

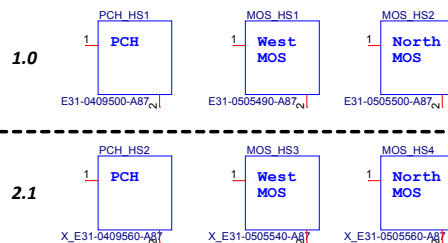


Marketing Name



PS0-07B2320-G37

HEATSINK



MICRO-STAR INT'L CO.,LTD			
MS-7B23			
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Custom	Manual Parts	1.0	
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